

Analog Signal Path Design Seminar

Training Manual and Reference Guide

2006



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RAEMIN WANG
SALES ENG.

781-221-4515

Raemin.Wang@nsc.com

Analog Signal-Path Design Seminar

2006

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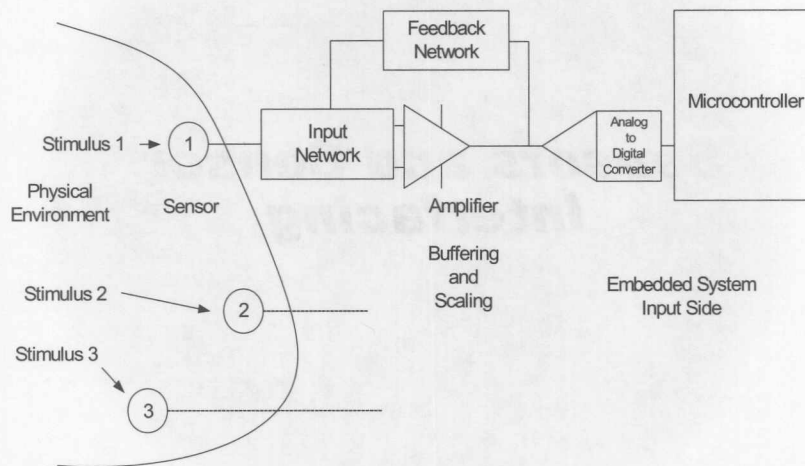
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Sensors and Sensor Interfacing

Many signal paths start with that most universal of analog components, the operational amplifier. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation, etc.) the modern op amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op amps often can combine many of these functions, because the transfer characteristic of an op amp is determined primarily by the external components connected around the op amp.

Physical Measurement System



Sensors are used to provide an input from the physical world, which is an analog environment, to control systems.

Sensors provide the interface from the physical environment to the electrical environment by converting the stimulus of interest into a voltage or current. In other words, there is a dependency between the physical measurement of interest and an electrical property of the sensor, and the sensor uses these dependencies to create an analog output signal.

For example, a thermocouple's output voltage will change as the temperature difference between the hot junction and cold junction changes. This is known as the Peltier Effect. For a Resistance Temperature Detector (RTD), the resistance to an electrical current changes as the temperature of the resistive element changes. This can be monitored by applying a constant (known) current to the sensor and measuring the change in voltage across the sensor as the temperature increases or decreases.

Most of the time the output of a sensor is not usable without additional buffering and scaling. This is the function of the amplifier and its input and feedback networks.

Sensor/Transducer Types

Property	Sensor/Transducer	Output
Force/ Pressure	Strain Gauge Piezoelectric	Resistance Voltage
Temperature	Thermocouple RTD (Resistance Temperature Detectors) Thermistor Silicon	Voltage Resistance Resistance Voltage/current
Acceleration	Accelerometer	Capacitance
Position	LVDT (Linear Variable Differential Transformer)	AC Voltage
Light Intensity	Photodiode	Current



Sensor Characteristics

- Active or passive
- Voltage or current output
- Source impedance
- Sensitivity
- Linearity
- Dynamic range
- Frequency response
- Common-mode signal components



All sensors will have a set of characteristics that will determine their suitability for a specific application. This list shows eight characteristics that are common and important.

An active sensor requires an excitation source in order to generate an output signal, while a passive sensor can generate an output signal directly.

The resistive measurement bridge is an example of an active sensor. It senses force by changing the resistance of one or more of the bridge's elements. The bridge is driven with a constant current source or a constant voltage source, and the output is a voltage proportional to the amount of force the sensor is being exposed to.

The thermocouple is a passive sensor, which will generate a voltage based on the temperature difference between the hot junction and the cold junction.

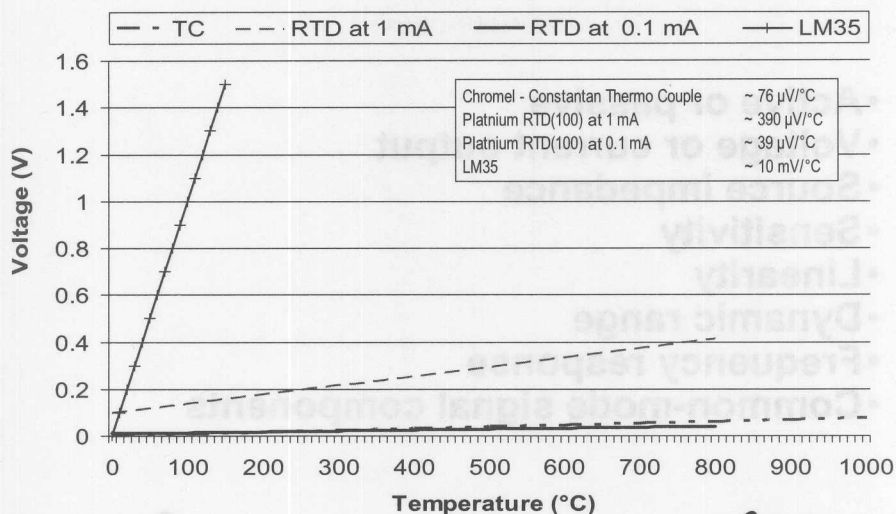
Typically, the voltage output sensor will interface with a voltage amplifier, while the current output sensor uses a transimpedance amplifier to convert the current to a voltage.

Examples of voltage output sensors include bridges, thermocouples, and pH electrodes. Photodiodes, photomultiplier tubes, and ion chambers are a few current output sensors.

High-impedance sensors will require amplifiers with very low input bias currents. This is because the amplifier's input bias current will load the sensor's output. For a high-impedance sensor, the amplifier must have bias currents in picoamps. Low-impedance sensors can use amplifiers with higher input bias currents, typically in nano-volts.

The sensitivity of a sensor specifies how much the output of the sensor changes for a unit change in the measured variable. Using a thermocouple and semiconductor temperature sensor as an example, a Chromel-Constantan thermocouple has a sensitivity of about $76 \mu\text{V}/^\circ\text{C}$, while a semiconductor temperature sensor has a sensitivity of $10 \text{ mV}/^\circ\text{C}$.

Temperature Sensor Sensitivity



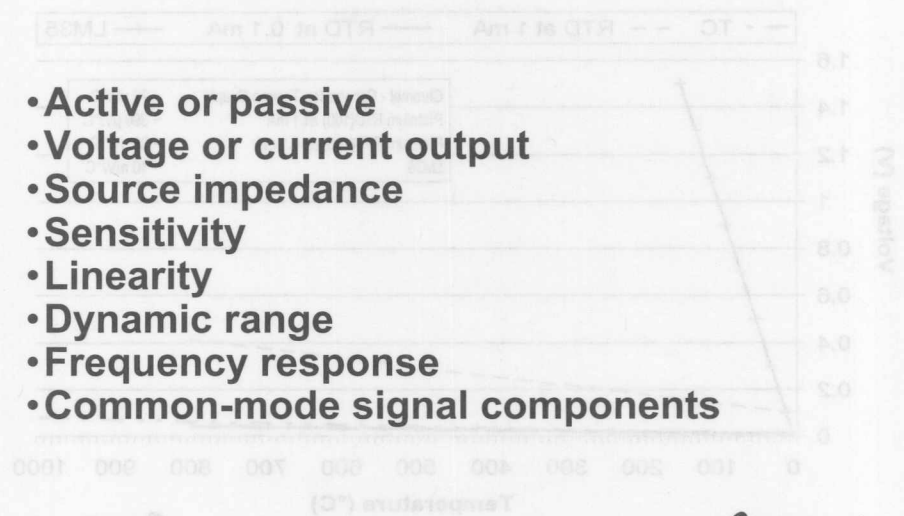
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Here are several examples for sensitivity of a sensor. The graph and table show the LM35, a semiconductor temperature sensor, a Chromel-Constantan thermocouple, and an RTD with two excitation current levels.

This shows how the sensitivity of an active sensor can be changed to meet specific requirements. A Platinum RTD (100) has 100Ω resistance at 0°C . With 0.1 mA excitation current, it has an output of about $39 \mu\text{V}/^\circ\text{C}$. At 1.0 mA excitation current, it has an output of about $390 \mu\text{V}/^\circ\text{C}$. The choice on which current to use could be based on other factors, such as minimizing the self-heating of the RTD.

Sensor Characteristics

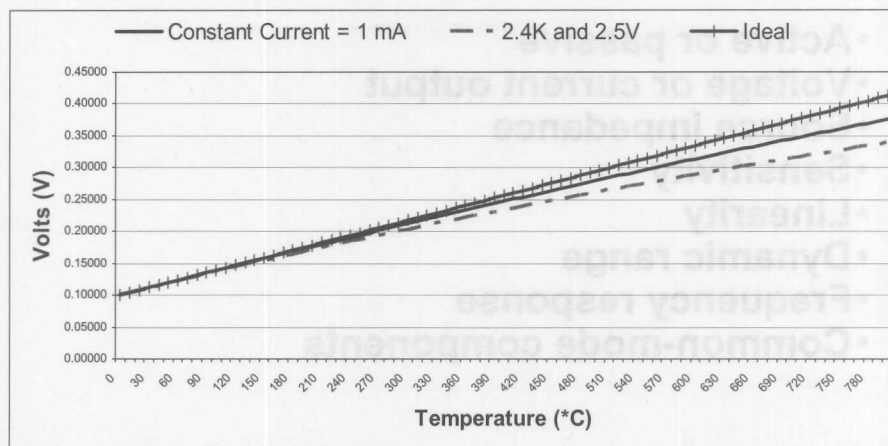
- Active or passive
- Voltage or current output
- Source impedance
- Sensitivity
- Linearity
- Dynamic range
- Frequency response
- Common-mode signal components



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Linearity specifies how close the sensor's transfer function is to a straight line. A linear transfer function is usually desirable because it simplifies converting the sensor's output to a useable form for monitoring the sensor output, or using it in a control loop. Some types of sensors such as RTDs, thermocouples, and bridges have linear, or close to linear, transfer functions. In contrast, other sensors, such as thermistors, have very non-linear transfer functions. Many non-linear transfer functions are most easily linearized after the Analog-to-Digital Converter (ADC) with a microcontroller performing this task by utilizing look-up tables.

Driving Active Sensors



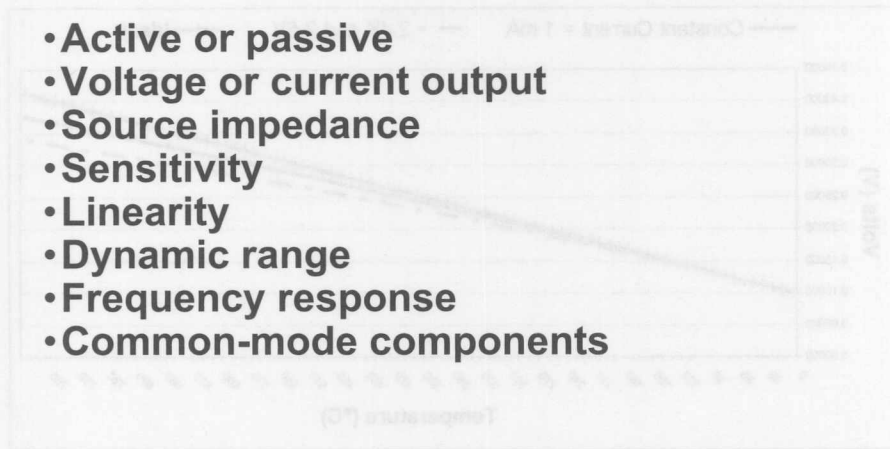
How an active sensor is excited also can affect its linearity. This graph shows the effect of using constant current excitation versus constant voltage excitation on a RTD.

The ideal (upper) curve is the slope of the RTD's transfer function extended to 800°C. The middle curve is the transfer curve of the RTD using 1 mA excitation current. This curve shows the small reduction in sensitivity of the RTD as the temperature increases.

The lower curve shows the results of using a constant voltage source and a series resistor to excite the RTD. The series resistance (2.4 k Ω) is sized to provide a 1 mA current at 0°C when the RTD's resistance is 100 Ω . The curve shows the second error term introduced by this type of excitation. As the resistance of the RTD increases, the RTD and the series resistor form a voltage divider that further decreases the linearity at higher temperatures.

Sensor Characteristics

- Active or passive
- Voltage or current output
- Source impedance
- Sensitivity
- Linearity
- Dynamic range
- Frequency response
- Common-mode components



The dynamic range of a sensor is the span of the stimulus for which a usable output is available. In other words, dynamic range defines the minimum to the maximum value of the physical phenomena that can be measured. Saturation or material failure could limit the dynamic range. Saturation is the rapid loss of sensitivity above or below a given level of the stimulus. Material failure sets a limit level of the stimulus beyond which the sensor will be damaged or destroyed. The thermocouple metals can melt if the temperature is too high, or a pressure transducer can rupture if the pressure being measured is too high. Some typical dynamic ranges are as follows:

Chromel – Constantan Thermocouple: Max Temperature $\sim 1000^{\circ}\text{C}$, Min Temperature $\sim -200^{\circ}\text{C}$
=> Dynamic Range = 1200°C

Semiconductor Temperature Sensor: Max Temperature $\sim 125^{\circ}\text{C}$, Min Temperature $\sim -40^{\circ}\text{C}$ =>
Dynamic Range = 165°C

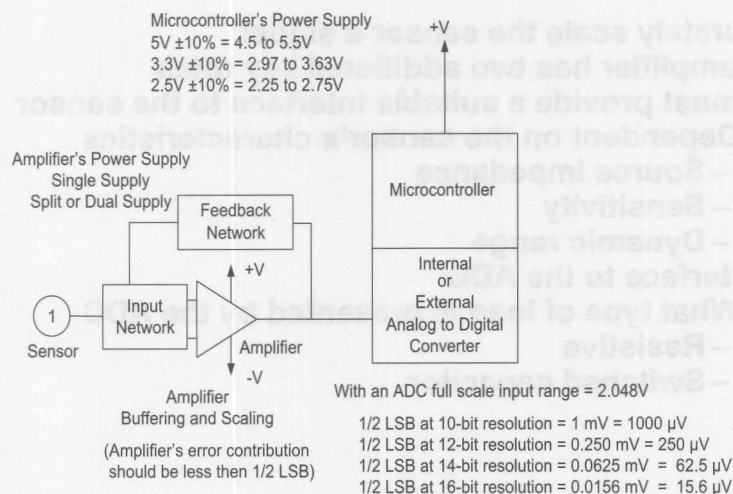
The signal frequencies of the sensor's output will depend on the type of measurement being made and can range from cycles per day for geophysical measurements to hundreds of megahertz for some types of radiation measurements. The required closed-loop bandwidth of the amplifier will depend on the frequency components of the sensor's output and the gain accuracy needed for those components.

Several types of sensors have small differential signals combined with large common-mode voltages. This large common-mode voltage must be removed to recover the data portion of the signal, or the small differential signal.

Bridge sensors will typically have the sensor's output signal riding on top of a common-mode voltage equal to about one half of the excitation voltage.

The current sensing resistor on a high-side current measurement circuit will have a common-mode voltage that is close to the supply voltage. The common-mode voltage must be removed to recover the sensor's signal.

Typical Embedded System Input



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Many of the microcontrollers used in embedded control systems are being forced to lower supply voltages as the semiconductor processes are migrating to smaller geometries. Digital logic supply voltages have decreased from 5V down to 3.3V and 2.5V. These voltages are now in the process of migrating to 1.8V and lower.

In the interest of power supply economics, analog amplifier supply voltages are following a similar trend. Recent analog semiconductor processes have also reduced the supply voltage ratings because of similar needs for smaller transistor geometries. These trends emphasize the need for DC accuracy because of smaller error budgets. Lower supply voltages reduce the dynamic range available for both amplifiers and ADCs. At the same time the required resolution of the signal-processing path is increasing.

A few years ago, a 12- to 14-bit ADC with a 10V full-scale input was considered good. Now, 16 bits and higher are expected with full-scale inputs of only 1 to 2V. This results in very low error budgets in the tens of microvolt range. This slide shows the typical error allocated to the amplifier's total system using a 2.048V ADC with different bit-accuracy requirements.

The Amplifiers' Roles

- **Accurately scale the sensor's signal**
- **The amplifier has two additional key roles**
 - **It must provide a suitable interface to the sensor**
 - **Dependent on the sensor's characteristics**
 - **Source impedance**
 - **Sensitivity**
 - **Dynamic range**
 - **Interface to the ADC**
 - **What type of load is presented by the ADC**
 - **Resistive**
 - **Switched capacitor**



Amplifying the sensor's output is often thought of as the primary function of the amplifier. As a result, it is common to think of the amplifier as the only factor that contributes to the precision of the system, but the sensor's output characteristics and ADC's input characteristics also have a significant effect on the total precision.

On the input side, each type of sensor has a unique set of parameters to consider. Characteristics such as source impedance, signal level, dynamic range, etc. are all part of the design constraints for the input and feedback network of the amplifier.

On the output side, the input characteristics of the ADC will affect the output of the amplifier. Most of the new ADCs have a switched capacitor input which presents a dynamic reactive load to the amplifier. The amplifier must be designed for settling quickly with this type of load or the ADC's input must be isolated from the amplifier's output.

When the ADC's input is connected directly to the output of the amplifier, the sampling capacitor in the ADC is connected to the amplifier's output. In this case, a charging current flows from the amplifier to the ADC. This current causes a momentary glitch that takes some time to settle. One way to minimize this effect is to slow down the sampling rate. This provides the amplifier with the time required to stabilize its output.

A second way to minimize the error caused by the switch capacitor is to have a capacitor connected to the ADC's input. This capacitor, much larger than the internal sampling capacitor, provides the charge needed to quickly charge the ADC's sampling capacitor. An isolation resistor also may be needed to isolate the additional load capacitance from the amplifier's output. Note that an isolation resistor will reduce the swing of the signal coming out of the amplifier since there is a voltage drop across the isolation resistor.

The amplifier, in conjunction with the input and feedback networks, has several tasks which include: Accurately scaling the signal to match the ADC's input voltage range, removing any common-mode components, and removing offsets that are inherent in the sensor's output.

The Amplifier's Requirements

- Precision sensor interface requirements
 - High open-loop gain
 - Low max offset voltage
 - Low offset voltage drift
 - Low noise
 - Voltage noise
 - Current noise
 - Low input bias current
 - High Common-Mode Voltage Rejection ratio (CMRR)
 - High Power Supply Rejection Ratio (PSRR)
 - Bandwidth (appropriate for the signal frequency)
 - *Effective signal bandwidth is a function of the amplifier's gain bandwidth, closed-loop gain, AND the measurement system resolution*



The amplifier's characteristics set the baseline for how much precision can be achieved.

The open-loop gain is a factor in the closed-loop gain error and should be as high as possible.

Offset voltage and offset voltage drift are multiplied by the noise gain of the feedback network and should be as low as possible.

The voltage noise and current noise should be small compared to the sensor's signal.

The input bias current should be low relative to the source impedances of the sensor and the input and feedback networks.

Several types of sensors have a common-mode voltage associated with their output that must be removed by the amplifier. Therefore, the Common-Mode Rejection Ratio (CMRR) of the amplifier should be as high as possible.

The power supply may be shared with active digital loads that will generate noise and ripple on power supply distribution circuit. The amplifier needs to have a high Power Supply Rejection Ratio (PSRR).

The amplifier's bandwidth must be calculated based on the precision required for the signal and is a function of the gain bandwidth and the closed-loop gain. The effective bandwidth drops rapidly as the required precision increases.

Offset Voltage and Drift

- **Definition of offset voltage**
 - Usually modeled as a voltage source on the non-inverting input
- **Definition of offset voltage drift**
 - Also known as offset voltage error
 - TCV_{OS} (temperature drift)
 - Life time drift
- TCV_{OS} : Variation of one part over temperature
- V_{OS} : General area that one part is expected to be in at room temperature



Offset voltage is one of the many characteristics of a “non-ideal” op amp. For an ideal op amp, the output voltage sits at mid-supply when there is no differential voltage applied between the inputs of an op amp. However, in reality, the output will be away from mid-supply value by a minimal amount. To correct this, a small amount of differential voltage needs to be applied between the inputs of the amplifier. The amount of differential voltage required between the inputs to bring the output back to mid-supply is referred to as input offset voltage or offset voltage.

Another way of looking at this: When there is no external differential voltage applied between the input of the amplifier, a small amount of voltage present in the circuit will be gained up by the amplifier’s gain and will show up on the output. So, if the amount of output offset voltage is known, we can calculate the input offset voltage using this relationship:

Input offset voltage = (output offset voltage) / (op amp’s gain)

The value of offset voltage changes under different conditions, or it “drifts.” The two main elements contributing to this drift are the passage of time and change in temperature. The term offset voltage drift usually refers to the temperature component.

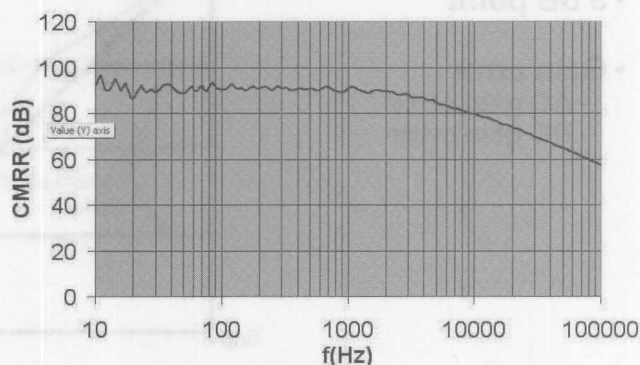
Input offset voltage is temperature dependent. This means the value of offset will be different at different temperatures. Offset voltage drift usually refers to the change in offset voltage per degree (Celsius) change in temperature. For general purpose op amps, this value is not very important since it is usually orders of magnitude smaller than the actual offset voltage. In precision amplifiers with very low offset voltages, drift is of special importance, since it could easily cause the offset voltage to double or triple at temperature extremes.

Input offset drift over time is the change in offset voltage per year (or any other specified time frame).

CMRR

- Definition of CMRR
- DC CMRR vs AC CMRR

CMRR VS frequency



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Op amps are designed so that they will respond only to a differential voltage between their two input pins. This means that for an ideal op amp, if the same voltage is applied to both input pins, the output will remain unchanged. This *common* signal between the two input pins is referred to as a *common-mode* signal. For an ideal op amp, common-mode signal does not change the output at all, meaning the op amp completely rejects this common-mode signal. In real op amps, parts of this signal will get through and show up on the output, while another portion of it will be rejected. The ability of an op amp to reject this common-mode signal is shown by ratio of the common-mode signal seen on the output to the ratio of the common-mode signal on the input. This is called Common-Mode Rejection Ratio (CMRR). An ideal op amp has a CMRR of infinity. Real op amps have finite CMRR values which are usually expressed in dB.

$CMRR = 20 \cdot \log[(\text{Change in offset voltage})/(\text{change in common mode voltage})]$ or equally:

$CMRR = 20 \cdot \log[(\text{differential gain of amplifier})/(\text{common mode gain of amplifier})]$

AC CMRR and DC CMRR: whenever there is a reference to CMRR, we are talking about DC CMRR or the ratio of differential gain to common-mode gain at zero frequency. The fact is that CMRR is heavily frequency dependent. As we know, the differential gain of an amplifier is relatively frequency independent and remains somewhat the same over a frequency range (it decreases a bit), while the common-mode gain of an amplifier increases with frequency (not a good thing) This means CMRR decreases over frequency.

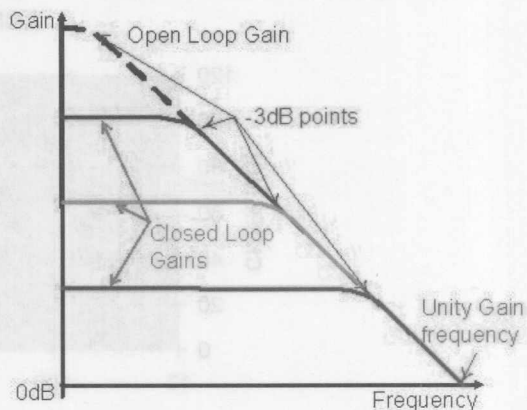
Gain Bandwidth

- **Gain-bandwidth product: conventional definition**

- **3 dB point**

- **Gain error**

- AC gain error
- DC gain error



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Gain-bandwidth product refers to the product of an amplifier's gain (in V/V) by the frequency at which that gain is achieved. This product remains constant for a voltage feedback op amp.

3 dB point refers to the point at which the amplifier's gain drops by 3 dB or it is 0.707 of its original value. For the most part, gain deviations of up to 3 dB have been deemed acceptable and have been working in most application circuits; however, we are using smaller and smaller signals everyday. On smaller signals, 0.707 of the original may already be too far away from our accuracy level needed. 0.707 of accuracy implies a margin of error of 0.293 (or 29.3%). In reality, with this margin of error, we cannot even have an accurate 4-bit converter! (4-bit converters have a maximum margin of error of 25%). This means we need to pick a frequency point much closer to the flat band with a much smaller margin of error. For instance, at the 1 dB point, we are only 10.87% away from the signal level. At 0.1 dB from flat band, we are 1.14% from the original signal level. Now, let's look at it from the other end. For a 12-bit converter, the maximum flat-band deviation is 0.002 dB!! (0.0244% error)

There are two main factors causing gain errors: one is a gain error due to frequency or AC-gain error, another is the result of the op amp being non-ideal and is referred to as the DC-gain error.

For an ideal op amp, gain remains constant until the roll-off point (the pole) and then the gain drops at 20 dB/dec or another multiple of this value (depending on number of poles present). However in real op amps, the gain starts drifting from the flat-band line much sooner. As we've discussed already, at the frequency corner, our gain has already been reduced by 3 dB.

DC-gain error of a non-ideal op amp: even without DC offset voltage, the output will be away from mid-supply. This is due to the fact that the gain of a non-ideal op amp is not infinite. This output voltage is modeled as DC-gain error.

Op Amp Error Sources

$$e_{id} = \frac{e_o}{A_{VOL}} + V_{OS} + (I_{B+})(R_{S+}) + (I_{B-})(R_{S-}) + \frac{e_{CM}}{CMRR}$$

- Major input referred error sources of an op amp
 $e_{id} = 0$ for ideal op amp
- Precision requires error terms to be small relative to the signal being processed
- A_{VOL} and CMRR are frequency dependent



This equation considers four of the major contributors to errors in op amps. The value e_{id} is the voltage between the two inputs of the op amp and is equal to zero for an ideal op amp.

The first term, e_o/A_{VOL} results from the finite gain of the amplifier. There must be a small differential voltage across the input to produce an output voltage. For example, if the output of an amplifier is 1.0 VDC and the open-loop gain is 100 dB, then the error voltage across the inputs is $1/105 = 10 \mu\text{V}$.

The second term, input offset voltage or V_{OS} , is a result of small imbalances on the differential input stage of the amplifier. The input offset voltage is also multiplied by the noise gain of the amplifier with its feedback. At high gains, the V_{OS} can become a large offset error.

The third and fourth terms result from the input bias currents in conjunction with any source resistance. Any current flowing into the amplifier's input will cause a voltage drop across the source resistance of $(I_B \times R_S)$. This has two effects. The first is to generate an apparent offset voltage at the input to the op amp if the equivalent source impedances on each input are not equal. The second is to add an error voltage to the signal that changes its apparent magnitude.

The last term brings in the effect of the common-mode voltage seen by the amplifier's input. The common-mode voltage, e_{CM} , is defined as the average voltage on the amplifier's inputs, $(e+ + e-)/2$. For example, if the common-mode voltage is 1V and the CMRR is 80 dB, the error on the amplifier's input due to the common-mode voltage is $1/104 = 100 \mu\text{V}$.

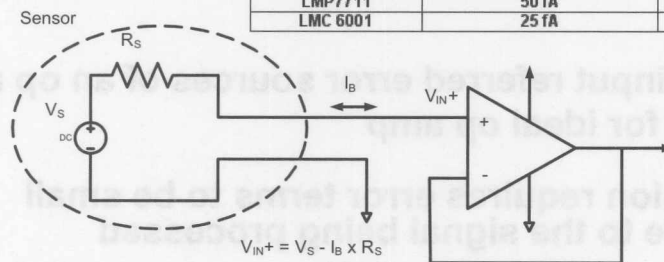
Each of the above error sources needs to be evaluated with respect to the specifications of the amplifier being considered.

As the frequency of the signal increases, the open-loop gain (A_{VOL}) and the CMRR will roll off with increasing frequency. This means a larger error term at higher frequencies.

Input Bias Current Induced Errors

Example: $R_s = 1\text{ M}\Omega$

Amplifier	Input Bias Current (typical)	Error
LM321	250 nA	250 mV
OP07	4 nA	4 mV
LMC6081	4 pA	4 μV
LMP7701	0.2 pA	0.2 μV
LMP7711	50 fA	50 nV
LMC6001	25 fA	25 nV



Error due to Amplifier's input bias current and the source resistance of the sensor.

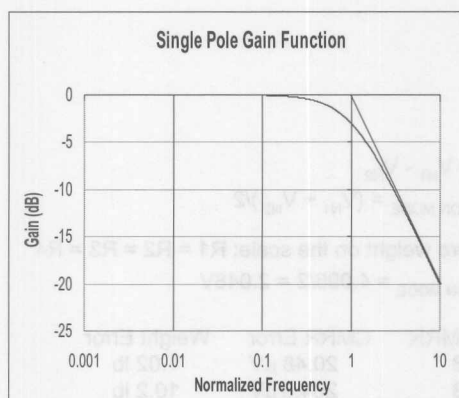
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Here is an example of the effect the input bias current has on the sensor's output. This sensor is a voltage output sensor with a source impedance of $1\text{ M}\Omega$. The table lists the typical input bias currents for five different amplifiers. The LM324 and OP07 are bipolar input amplifiers, while the LMC6081, LMP7701, LMP7711, and LMC6001 are FET input amplifiers.

The bipolar input amplifiers have a large error relative to the FET input amplifiers. It is also useful to note that precision amplifiers are available with guaranteed very low, sub pico-amp input bias currents. Some examples include the LMP7701, LMP7711, and LMC6001.

*CMOS bias current
doubles for every 10°C. change (increase)*

Closed-Loop Bandwidth



System Resolution	Normalized Bandwidth for < 1/2 LSB Error
8-bit	0.062592
9-bit	0.044227
10-bit	0.031261
11-bit	0.022101
12-bit	0.015626
13-bit	0.011049
14-bit	0.007813
15-bit	0.005524
16-bit	0.003906

What bandwidth is available?

Example:

LMP2011: GBW = 3 MHz

At a gain of 20 BW = 150 kHz

For 12-bit accuracy

max signal frequency is

$0.0156(150 \text{ kHz}) = 2.34 \text{ kHz}$



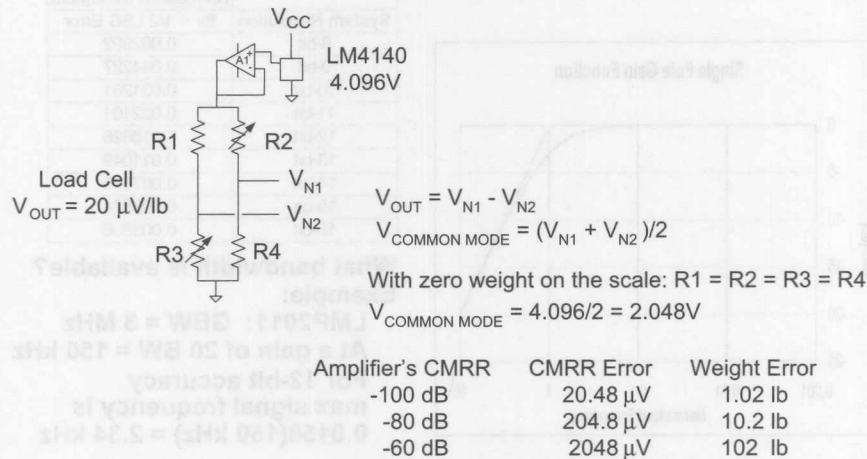
This graph and table is a method for estimating the effective bandwidth of an amplifier given its gain bandwidth, closed-loop gain, and the resolution of the system.

The normalized bode plot represents the specification given in the amplifier datasheet which is the gain bandwidth (GBW). Typically, the GBW is the frequency where the amplifier's output is down by 3 dB. The -3 dB point represents a 29.3% error ($100\% - 70.7\%$). This can be interpreted as the bandwidth needed to maintain a specified precision is substantially less than the -3 dB frequency.

The table shows how much bandwidth is available for a given precision.

Using the LMP2011 with a 3 MHz GBW as an example: at a closed-loop gain of 20 and a 12-bit accuracy requirement, the effective bandwidth of the amplifier is only 2.34 kHz. If the accuracy is increased to 16 bits, the effective bandwidth is only 0.59 kHz.

CMRR Error Example



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In this example, the effect of the amplifier's CMRR and its contribution to the system's error is shown. This is a resistive bridge being used on a load cell to measure weight. The sensitivity of the load cell is 20 $\mu\text{V/lb}$ and has a 4.096 excitation voltage. The common-mode voltage at the bridge's output is 2.048V. The table shows the error with three values of CMRR. Even with 100 dB of CMRR there is an error of about 1 lb.

Temperature Sensors

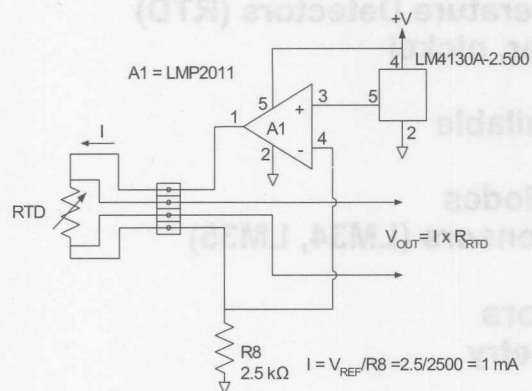
- **Common contact temperature sensors**
 - **Resistance Temperature Detectors (RTD)**
 - **Platinum, copper, nickel**
 - **Thermocouples**
 - **Many alloys available**
 - **Thermistors**
 - **Semiconductor diodes**
 - **Semiconductor sensors (LM34, LM35)**
- **Non-contact sensors**
 - **Infrared thermometry**



Temperature is one of the most commonly measured properties and a variety of sensors have been developed for this. Of these, the RTD and the thermocouple are widely used in industrial processes.

The next several slides show an RTD and a thermocouple amplifier circuit.

Resistance Temperature Detector



- Current source design
- low drift components
- RTD self-heating (I^2R)
- thermal impedance
- For a temperature range of 0°C to 600°C, sensor resistance: 100Ω to 329.64Ω
- V_{OUT} : 0.1 to 0.32964V (Plus 2.5V CMV)
- Scale signal to 2.5V
 $A_V = 2.5 / 0.32964 = 7.58$
 (Includes the non-zero signal offset)



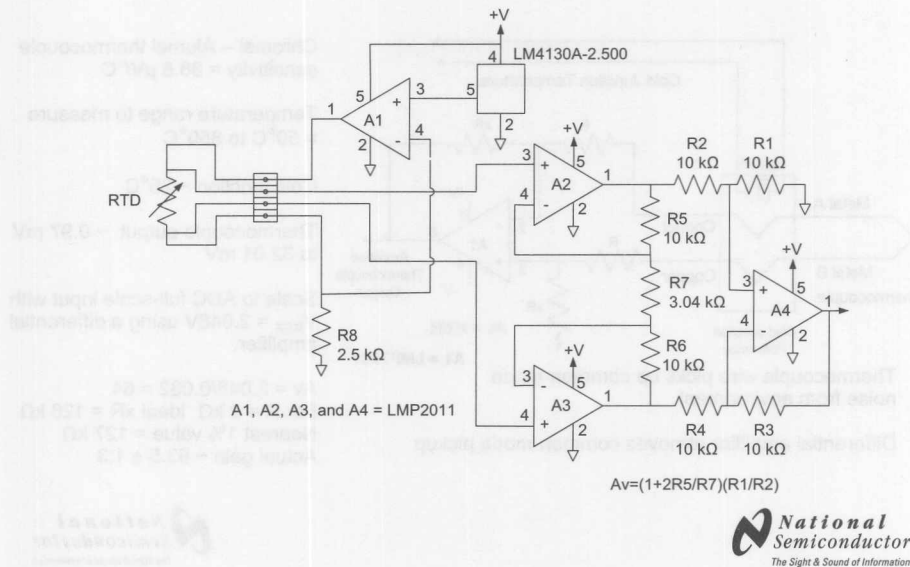
Here is the 1 mA constant current excitation for the RTD. The LM4130A-2.500 is the reference for the current source and the 2.5 kΩ resistor is the current sense resistor. The combination of the LMP2011, the LM4130, and a precision 2.5 kΩ resistor creates an accurate and stable current source.

The LMP2011 is a good operational amplifier choice for this application. The LMP2011 has very low input offset voltage of less than 1 μV, with an offset voltage drift of only 15 nV/°C. These impressive specifications, along with the low input voltage noise of only 35 nV/√Hz, mean that the LMP2011 will introduce minimal noise to the overall system, allowing for a much more accurate measurement.

The RTD is shown with a 4-wire Kelvin connection. The current flows through the force leads while the sense leads, which are precisely connected to the active resistor element, connect the voltage that is across the resistor to the signal amplifier.

Note that the RTD signal has three components: the temperature signal represented by change in resistance, an offset voltage due the non-zero resistance at the starting temperature, and a common-mode signal of 2.5V due to the current sense resistor.

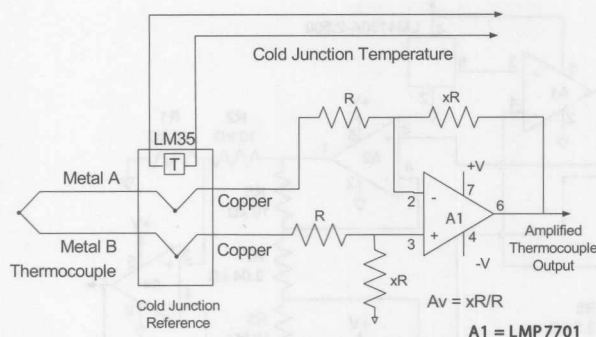
RTD with Amplifier



The RTD signal is being scaled to 2.5V full scale and the required gain is 7.58. See the previous slide for the calculation. Three LMP2011 amplifiers are used to build an instrumentation amplifier with a fourth LMP2011 used to buffer the reference voltage. The LMP2011 provides a very high CMRR and low offset voltage and drift.

The LMP2011 is the single amplifier in a family which includes the LMP2012 dual and LMP2014 quad precision amplifiers. Any combination of the single, dual, or quad amplifiers can be used in this application, depending on available board space.

Thermocouple Interface



Thermocouple wire picks up common-mode noise from environment

Differential amplifier removes common-mode pickup

Chromel – Alumel thermocouple
sensitivity = $38.8 \mu\text{V}/^\circ\text{C}$

Temperature range to measure
= 50°C to 850°C

Cold junction $\sim 25^{\circ}\text{C}$

Thermocouple output ~ 0.97 mV
to 32.01 mV

Scale to ADC full-scale input with $V_{REF} = 2.048V$ using a differential amplifier.

$$A_v = 2.048 / 0.032 = 64$$

For $R = 2 \text{ k}\Omega$ ideal $xR = 128 \text{ k}\Omega$

Nearest 1% value = 127 k Ω

Actual gain $\sim 63.5 \pm 1.3$



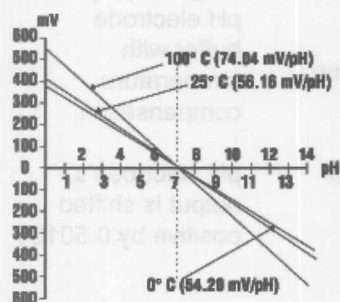
Here is an example of a thermocouple amplifier. The thermocouple has a low source impedance so a single differential amplifier can be used. The differential amplifier is used to remove common-mode noise that the wires pick up from the environment.

The thermocouple has a full-scale output of 32 mV in the temperature range of interest, and it is desired to scale this to 2.048V full scale. The required ideal gain is 64.

Also shown is an LM35 being used to measure the cold-junction reference temperature. The amplified thermocouple signal and the LM35 output go to an ADC for conversion.

The LMP7701 is a single precision operational amplifier with very high DC precision, offset voltage of only 37 μV , with an offset drift of 1 $\mu\text{V}/^\circ\text{C}$, and a GBW of 2.5 MHz. This amplifier can be used in higher gain settings without losing accuracy or running out of bandwidth.

pH Electrode Interface



pH Electrode Transfer Function

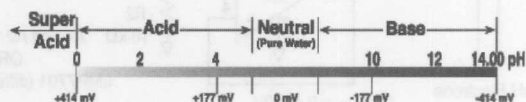


Source Impedance = 9 M Ω

Maximum output voltage range
= -0.51828 to 0.51828 V
Requirement

Shift signal: 0.0V sensor signal
= 1/2 ADC input range

Scale signal: 1.03656V sensor signal range
to ADC input voltage range

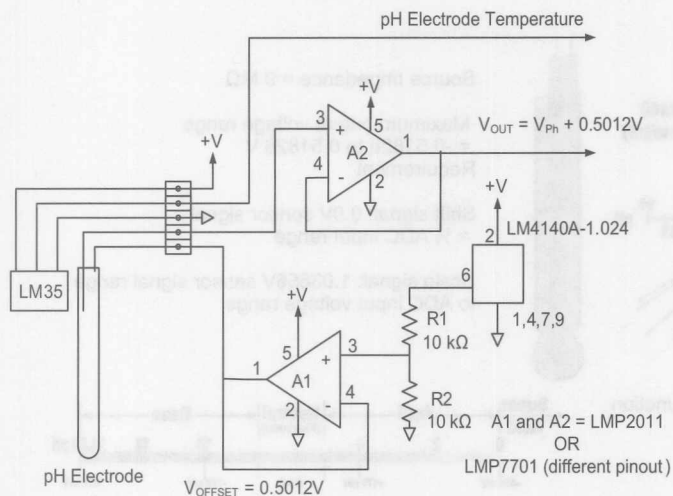


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pH electrodes are used to measure the pH of a solution. The graphs above show the physical relationship between the pH of a solution and the output voltage of the pH electrode and its temperature dependence. The source impedance of the pH electrode is typically $10^6\Omega$ to $10^7\Omega$. For most practical uses, the pH electrode must be buffered before driving the cable to the measurement instrument. Additionally, to obtain an accurate measurement of pH, the temperature of the pH electrode must be known.

Note that the output signal is bipolar and will require level shifting to be used in a single supply system.

pH Electrode Interface Ex1



Single supply
pH electrode
buffer with
temperature
compensation

pH electrode's
output is shifted
positive by 0.5012V



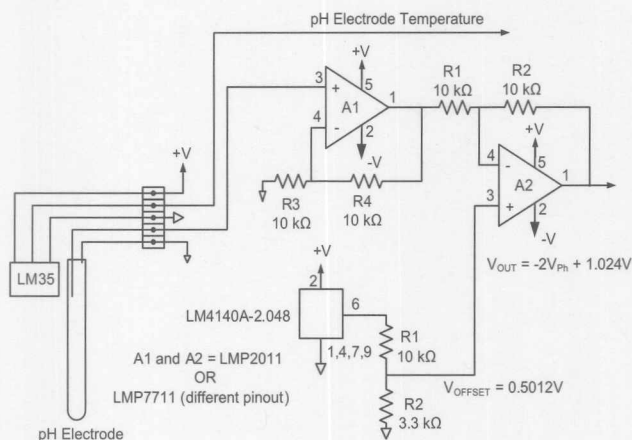
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The output voltage of a pH electrode is high enough to use without additional amplification. In this single-supply circuit, the pH electrode is offset by a little more the 0.5V by amplifier A1. The second amplifier, A2, buffers the output of the pH electrode and drives the ADC. This circuit shifts the bipolar pH electrode signal to a unipolar signal for use in a single supply system.

The LM35 is used to measure the temperature of the electrode so a temperature corrected pH measurement can be taken.

Both the LMP7701 and LMP2011 are excellent choices for this application.

pH Electrode Interface Ex2



Dual supply
pH electrode
amplifier with
temperature
compensation

pH electrode's
output is amplified
by two and shifted
positive by 1.024V

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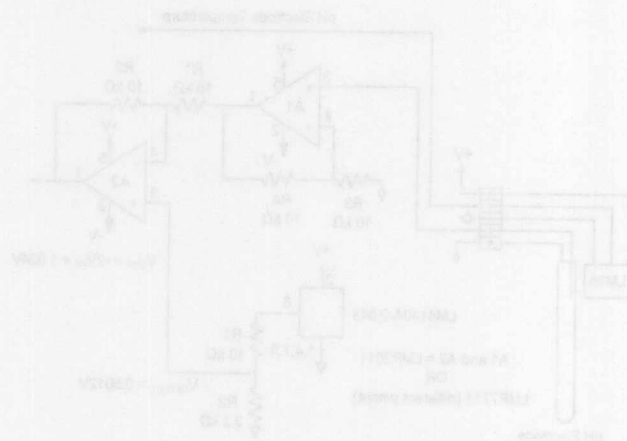
In this circuit, the pH electrode is amplified and level shifted. The amplifier A1 has a gain of two in addition to providing a high input-impedance buffer to the pH electrode. Amplifier A2 does the level shifting function so the signal is unipolar.

LMP7711 is a precision single operational amplifier with a high gain bandwidth of 17 MHz and very low voltage noise of $5.8 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz with a corner frequency at 400 Hz. These characteristics along with an input offset voltage of only $20 \text{ } \mu\text{V}$ and offset drift of $1 \text{ } \mu\text{V}/^\circ\text{C}$ make this op amp ideal for precision applications. Both the LMP2011 and LMP7711 are excellent for this application.

The LM35 is used to measure the electrode temperature.

pH Electrode Interface Ex2

pH electrode
 amplifier with
 temperature
 compensation
 pH electrode's
 output is amplified
 by two and shifted
 positive by 7.024V



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 Application Note

In this circuit, the pH electrode is amplified and level shifted. The amplifier A1 has a gain of two in addition to providing a high input impedance buffer to the pH electrode. Amplifier A2 does the level shifting function so the signal is unipolar. LM2771 is a precision single operational amplifier with a high gain bandwidth of 17 MHz and very low voltage noise of 2.5 nV/√Hz at 1 kHz with a corner frequency at 400 Hz. These characteristics along with an input offset voltage of only 30 μV and offset drift of 1 μV/°C make this op amp ideal for precision applications. Both the LM2771 and LM2771 are excellent for this application.

The LM2771 is used to measure the electrode temperature.

Stability Issues

Oscillators don't!
Amplifiers do!

It is possible to look at the stability of a closed-loop amplifier (or any feedback circuit) by analyzing the behavior of the forward path ("A") or open-loop gain plus feedback (feedback factor) as shown above.

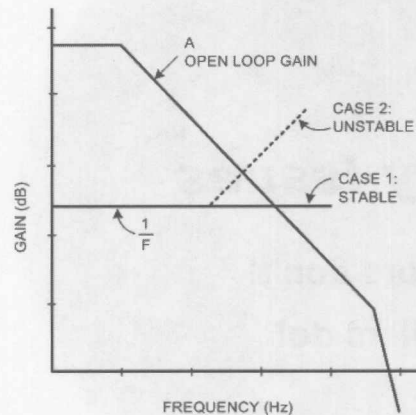
As you may recall, stability at any frequency means that the phase is a gain of 360° around the loop with 180° of phase shift at that frequency. So it is necessary to see that stability involves both the forward path (A) and the feedback path (B) relationship (both gain and phase). The closed-loop transfer function denominator is both inverting and non-inverting configurations, $1 + A\beta$, where both A and β are complex numbers (magnitude and phase) and frequency dependent. It is easy to understand that having the denominator represent zero is a bad thing and in most real circuits, when this happens, the circuit starts two oscillations.

Mathematically, this is the same as the term $A\beta$ becoming 1 in value, because $A\beta$ with a value of 1 and 180° phase is the same as a real number of value -1. If $-A\beta = 1$ at a frequency where $A \sim 1/\beta$, oscillation can occur.

This means that the stability condition stated above is nothing but observing the phase shift around the loop when the two curves (A and β) intersect and when β starts to rise from 180° of phase shift, the denominator curve is not out and through the (forward) OK. Looking at the above diagram, with A and β plotted, a single pole or zero or any frequency produces a 45° phase shift at that frequency, a 90° phase shift and a 180° phase change in the sign of the curve above that frequency. It is easy to develop the phase information based on the gain plot shown above. In a nutshell, if the two curves approach each other at a rate of constant gain, then the likelihood that there is chance of oscillation. The following table explains further. For the plot shown, Case 1 will be stable and Case 2 will not.

Let's see why that is.

Graphical Stability Analysis 1



- **A** and **1/F** plots and where they intercept each other include all information necessary to say if a closed-loop circuit is stable or not and to what degree!

- **Case 1** is "stable" and **Case 2** is not.



It is possible to look at the stability of a closed-loop amplifier (or any feedback circuit) by analyzing the behavior of the forward path ("A" or open-loop gain plot) alongside the feedback factor (1/F) as shown above.

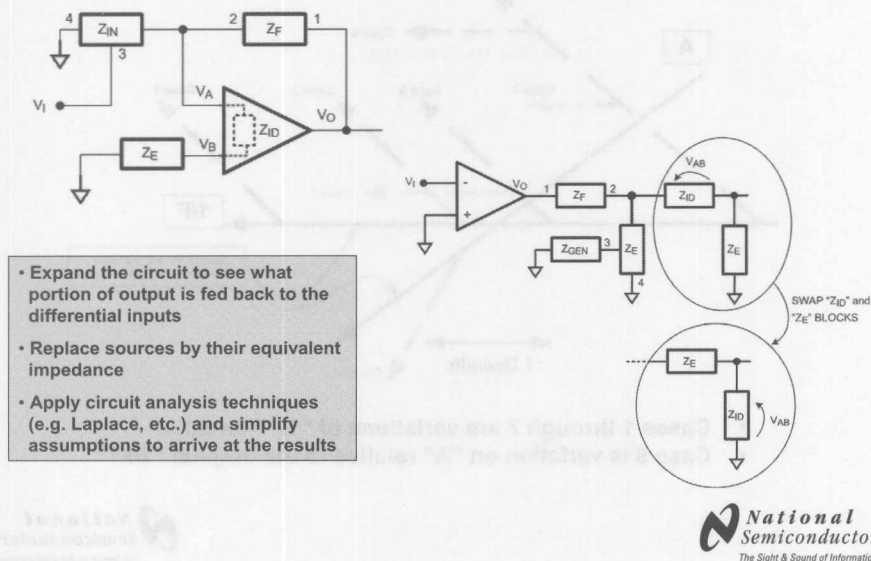
As you may recall, instability at any frequency occurs when there is a gain of ≥ 1 around the loop with 180° of phase shift at that frequency. So, it is reasonable to see that stability involves both the forward path (A) and the feedback path (F) information (both gain and phase). The closed-loop transfer function denominator, in both inverting and non-inverting configurations, is $1 + AF$, where both A and F are complex numbers (magnitude and phase) and frequency dependent. It is easy to understand that having the denominator approach zero is a bad thing and in most real circuits, when this happens, the circuit breaks into oscillations.

Mathematically, that is the same as the term AF becoming 1 in value, because AF with a value of 1 and 180° phase is the same as a real number of value -1. If $1 + AF = 0$ at a frequency where $A = 1/F$, oscillations can occur.

This means that the stability condition stated above is nothing but observing the phase shift around the loop when the two curves (A and 1/F) intercept each other. If there is less than 180° of phase shift, the oscillation criteria is not met and things are (almost) OK. Looking at the above diagram, with A and 1/F plotted, a single pole or zero at any frequency produces a 45° phase shift at that frequency, a 90° phase shift, and a 20 dB/decade change in the slope of the curve above that frequency. It is easy to decipher the phase information based on the gain plots shown above. In a nutshell, if the two curves approach each other at a rate of closure greater than 40 dB/decade, then there is chance of oscillation. The following foils explain further. For the plot shown, Case 1 will be stable and Case 2 will not.

Let's see why that is.

Determining the Feedback Function



Let's look and see how the feedback factor is determined for an arbitrary circuit.

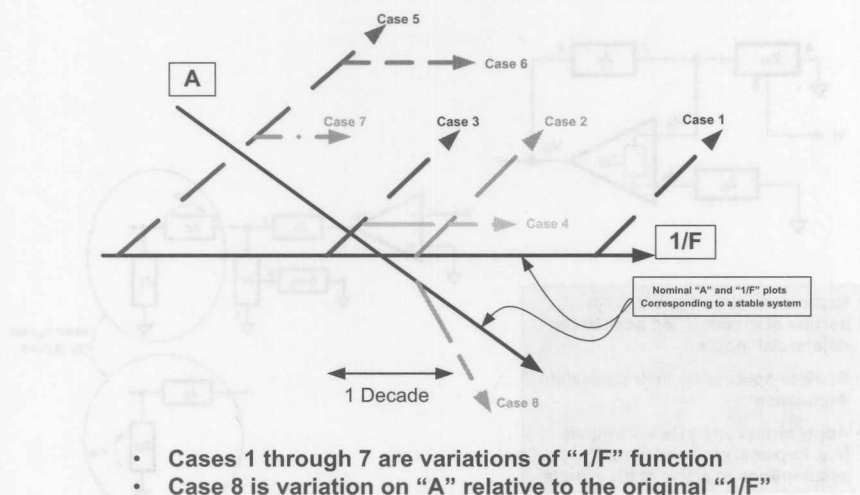
The $1/F$ function referred to in the last slide is the ratio of what is fed back to the amplifier's inputs from the amplifier's output. In the diagram shown above to the left, that would be $F = (V_A - V_B)/V_O$.

To be able to do stability analysis, graphical or otherwise, it is essential to be able to come up with the F function expression. It is easier to do so by expanding out the whole circuit as is done here to the right. Done this way, you can see that coming up with F is an exercise in circuit analysis techniques. Note that when doing this:

- The inputs have been removed and replaced by their equivalent impedance (Z_{GEN} in this case).
- This analysis will also work for two terminal devices.
- The calculation for F is for stability analysis only. This value will not arrive at the correct closed-loop gain if substituted inside the overall transfer function.

Note that the expanded schematic is further simplified by swapping the position of Z_{ID} and Z_E blocks. This change does not significantly alter the final result (because of an op amp's high CMRR) and thus simplifies the analysis as the voltage across Z_{ID} is now ground-referenced.

Graphical Stability Analysis 2



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Notice that until now we have not done anything with the phase information of A or 1/F. That is, because the magnitude Bode approximations contain a lot of information about phase within them.

Each break in the A or 1/F magnitude plot corresponds to up to 90° of phase shift (either positive or negative). Assuming the A and 1/F plots look as shown for the case shown labeled as “nominal,” there will be complete stability. The horizontal axis shows is of course log frequency. The reason is that at the frequency of intercept, “A” dominant pole (not shown) would have contributed to 90° of phase lag and the “1/F” is flat, corresponding to no additional phase shift. So, assuming that the op amp’s higher order poles are at least one decade beyond the intercept point, this is a super stable case with up to 90° of phase margin. Most systems will not behave this way, and even if they did, they will have non-optimized bandwidth.

The other cases shown will have other stability results. We will explore them in the following slides.

Stability Case Study 1

Table 2: Stability Summary for the Cases Shown

Notes:

IP: Intercept point_ Referring to the frequency where A and 1/F intercept

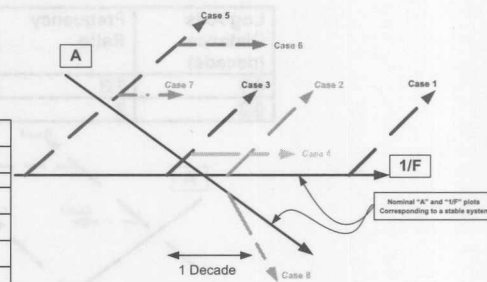
FB: Feedback

PM: Phase Margin

Case #	Condition	Estimated Loop Phase (deg.)	Estimated PM (deg.)	Comment
1	No FB phase shift	90	90	Overdamped response
2	FB pole at 0.3 decade above IP	$90 + 27 = 117$	63	Stable
3	FB pole at 0.3 decade below IP	$90 + 63 = 153$	27	Close to instability
4	FB pole at 0.3 decade below and FB zero at 0.1 decade above IP	$90 + 63 - 38 = 115$	65	Stable
5	FB pole at more than 1 decade below IP	$90 + 90 = 180$	0	Unstable
6	FB pole at more than 1 decade below and FB zero at more than 1 decade above IP	$90 + 90 - 0 = 180$	0	Unstable. The FB zero is too far from IP point
7	FB pole at more than 1 decade below & FB zero at 0.1 decade above IP	$90 + 90 - 38 = 142$	38	Close to optimum PM
8	"A" pole at 0.5 decade above IP	$90 + 18 = 108$	72	Stable

Table 1: Conversion of Log Frequency Distances to Phase Angle for Reference

Log Axis Distance (decade)	Frequency Ratio	Total Phase below pole (zero)	Total Phase above pole (zero)
0	1.0	45	45
0.1	1.3	38	52
0.3	2	27	63
0.5	3	18	72
0.7	5	11	79
0.9	8	7	83
1.0	10	6	84
2	100	0.6	89



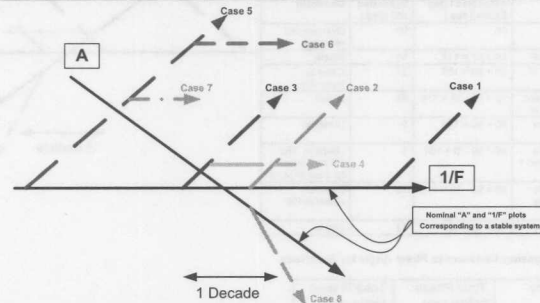
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The table to the top, Table 2, shows the stability result for each case shown. It uses Table 1, bottom, to estimate the phase due to each inflection point (pole or zero) in order to arrive at the total phase shift around the loop at the Intersection Point (IP). Note that in each case, IP refers to when the A plot intercepts the 1/F plot.

Let's take one of the cases shown and see if we can reconstruct the values shown in Table 2.

Stability Case Study 2

Log Axis Distance (decade)	Frequency Ratio	Total Phase below pole (zero)	Total Phase above pole (zero)
0.1	1.3	38	52
0.3	2	27	63



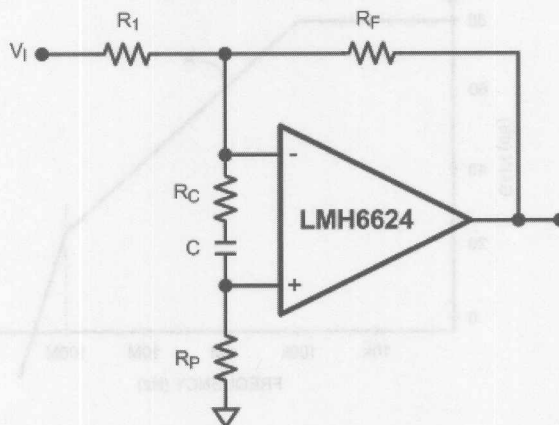
Case #	Condition	Estimated Loop Phase (deg.)	Estimated PM (deg.)	Comment
4	FB pole at 0.3 decade below and FB zero at 0.1 decade above IP	$90 + 63 - 38 = 115$	65	Stable



For example, let's take Case 4, which is highlighted from Tables 1 and 2 of the previous slide for clarity:

As you can see, there are two inflection points on the 1/F plot for this case. First is a zero at about 0.3 decades below IP and second is a pole at about 0.1 decade above IP. Note that it is assumed that the 1/F plot is flat all the way down to DC below the first inflection point. The A plot sloping downward at -20 dB/decade is indicative of one pole prior to IP. Taking a look at Table 1 shows that the first 1/F zero will cause an additional phase shift of 63° at IP frequency. However, the 1/F pole at 0.1 dB above IP is close enough to have its own effect at IP. Looking up 0.1 decade in Table 1 shows that this pole will have a phase reducing effect of 38°. Taken together, you will see the total loop phase is 115° corresponding to about 65° of Phase Margin (PM).

Compensation Example 1 (Schematic and Compensation Defined)

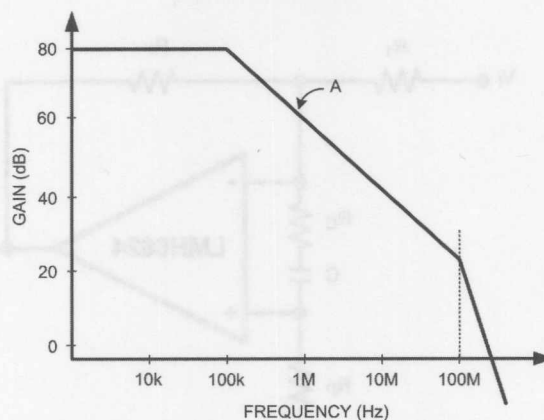


Let's put to use what we have already discussed in a real application.

The LMH6624, a very low-noise, high-speed op amp, is used in an inverting unity-gain application. However, the LMH6624 is optimized for bandwidth and is internally compensated for closed-loop gains larger than 20 dB (10 V/V). A well-known technique that allows the user to compensate a non-unity gain stable part (such as the LMH6624) for stable operation at any gain is the lead-lag compensation shown (due to the action of R_C , C , and R_P). The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is 0 dB.

Let's see if we can take advantage of this technique using the LMH6624 at a gain lower than the recommended minimum gain stated in the datasheet.

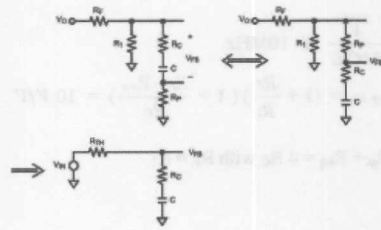
Compensation Example 1 (LMH6624 Data)



The LMH6624 datasheet shows the open-loop gain/phase that is invaluable in this situation where we have to customize the circuitry around the part for stability. We will take advantage of the data shown here in its simplified form and labeled as A. As you can see, the LMH6624 has a dominant pole at around 100 kHz and a second one falls at about 100 MHz. Just looking at the plot of A, you would be able to say that if the device is run at gains below about 20 dB (10 V/V), there is the possibility of instability, even if the feedback circuit adds no additional phase shift. At exactly 20 dB, the phase margin will be around 45° (90° due to the first pole and 45° for the 100 MHz pole).

To tackle this problem using the techniques discussed so far, it is imperative that the “1/F” function needs to be obtained before anything else.

Compensation Example 1 (Feedback Analysis)



$$V_{Th} = \frac{R_1}{R_1 + R_f} V_O$$

$$R_{Th} = R_p + \frac{(R_1)(R_f)}{R_1 + R_f} = R_p + R_{eq}$$

$$\text{where: } R_{eq} = \frac{(R_1)(R_f)}{R_1 + R_f}$$

$$F = \frac{V_{FB}}{V_O} = \left(\frac{R_c + 1/sC}{(R_c + 1/sC) + R_{Th}} \right) \left(\frac{V_{Th}}{V_O} \right)$$

$$F = \left(\frac{1 + sCR_c}{1 + sC(R_c + R_p + R_{eq})} \right) \left(\frac{R_1}{R_1 + R_f} \right) \left(\frac{V_{Th}}{V_O} \right)$$

$$\frac{1}{F} = \left(1 + \frac{R_f}{R_1} \right) \left(\frac{1 + sC(R_c + R_p + R_{eq})}{1 + sCR_c} \right)$$

$$f_z = \frac{1}{2\pi C(R_c + R_p + R_{eq})}$$

$$f_p = \frac{1}{2\pi CR_c}$$

$$\frac{1}{F} \Big|_{f=0} = 1 + \frac{R_f}{R_1} \quad \frac{1}{F} \Big|_{f=\infty} = \left(1 + \frac{R_f}{R_1} \right) \left(1 + \frac{R_p + R_{eq}}{R_c} \right)$$



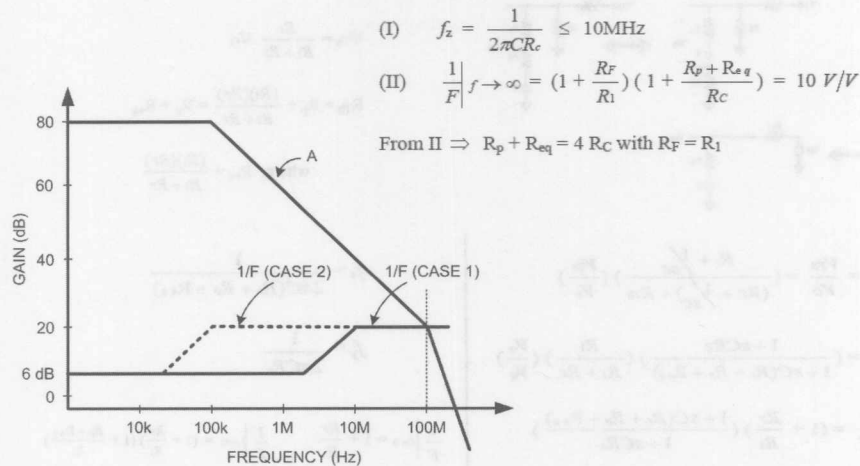
Therefore, we will expand the feedback path as we had already discussed, as shown here. In addition, we will swap the position of R_p and R_c , C combination in order to get the quantity in which we are interested, the voltage across the R_c to C combination, ground-referenced to ease calculations.

Calculation of F (and eventually $1/F$) becomes a task of solving for the voltage across the R_c , C combination as a function of the output voltage, which we have done here using Laplace transform arithmetic. Note that to simplify the analysis, the Thevenin equivalent concept is employed making the calculation one of a simple voltage divider, as shown.

Eventually, the $1/F$ function is calculated and its two inflection points are identified in the lower right-hand corner.

Armed with this information, once the component values are known, the $1/F$ gain Bode plot is easily constructed. However, this example is not one of analysis, but rather it is a case that involves synthesis. The information about $1/F$ will be used in the next slide to allow good engineering judgment in choosing the compensation components for optimum results.

Compensation Example 1 (Component Value Derivation 1)



This is the open-loop gain plot of the LMH6624 with the 1/F function superimposed on top of it for stability analysis.

- In plotting 1/F, here are the criteria or requirements applied:

It is desirable to have the IP occur at 100 MHz, which is the op amp's second pole to get about 45° of phase margin.

- 1/F pole must be at least one decade below IP so that the required 45° phase margin is not degraded. Recall that if the op amp's second pole at 100 MHz and the 1/F zero are less than one decade apart, they will have some interaction and the phase margin will be less than 45° since the stability improving effect of the 1/F has not taken full effect by IP.
- 1/F low frequency value is fixed by $1 + R_F/R_1$, which in this case will be 2 V/V or 6 dB.
- As derived in the previous slide, 1/F will have a lower frequency zero and a higher frequency pole.

The criteria/conditions above, which are stated mathematically to the right, will result in the 1/F shape shown. You will notice that two cases for 1/F are shown. To minimize output noise, case 1 is the preferred 1/F plot, as it minimizes the op amp's input-noise voltage gain increase due to the zero in the 1/F function. This may or may not be important for the application, but it is something to note here. We will assume it to be of importance in this case. In addition, it is always the best practice to preserve loop gain as much as possible, and case 1 again does that better than for example case 2. So, that means we would like to set the 1/F zero at exactly one decade below 100 MHz (or 10 MHz). At this point, we are ready to pick some component values and derive the other ones to satisfy these requirements.

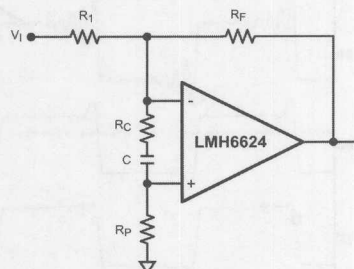
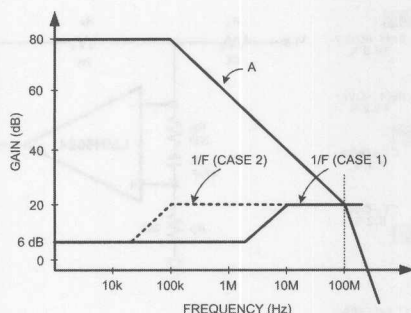
Compensation Example 1 (Component Value Derivation2)

$$(I) \quad f_z = \frac{1}{2\pi C R_c} \leq 10 \text{ MHz}$$

$$(II) \quad \left| \frac{1}{F} \right|_{f \rightarrow \infty} = \left(1 + \frac{R_f}{R_1} \right) \left(1 + \frac{R_p + R_{eq}}{R_c} \right) = 10 \text{ V/V}$$

From II $\Rightarrow R_p + R_{eq} = 4 R_c$ with $R_f = R_1$

Design #	C (pF)	R _c (Ω)	R _p (Ω)	Comments
1	100	160	-	R _p negative because R _c is too low
2	47	340	360	
3	27	590	1.36k	
4	10	1.6K	5.4k	



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Many values of C , R_c , and R_p can be picked to satisfy both conditions stated in Equations (I) and (II) above.

To reduce the effect of shunt capacitance across critical resistors for high-frequency operation, let's keep the values of R_f below 2 kΩ. Note that R_f and R_1 are equal for a gain of -1. If $R_f = R_1 = 2 \text{ k}\Omega \Rightarrow R_{eq} = 1 \text{ k}\Omega$.

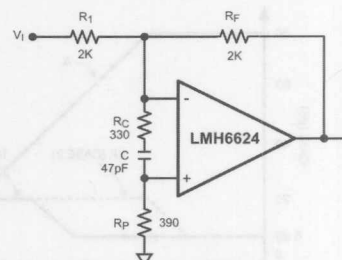
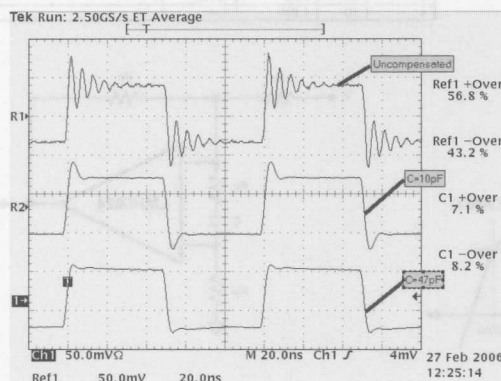
In the table shown, you will see that one way to do this would be to start with a value for C and then from that, you would be able to determine the R_c that would put the 1/F zero at 10 MHz (or Equation I above). With C and R_c known, Equation II dictates the value of R_p to meet the IP gain requirement.

As you can see, starting with $C = 100 \text{ pF}$ results in a value for R_c that is too low to result in a real value for R_p . So, to increase R_c , it is obvious that C would have to decrease. Therefore, you see that subsequent attempts all result in real values of R_p and are, therefore, all viable. Now the question is, which of these values to choose? Obviously, Design 2 through 4 will all work. However, it is best to avoid extreme values. In this case, Design 4 is probably not the best choice because with C at 10 pF, you start approaching parasitic capacitance levels on the board and active components. So, both Designs 2 and 3 are viable first choices.

Because compensation almost always requires some sort of "fine tuning" to arrive at the most optimum results, it is always desirable to have a means for varying it. You will note that varying C will move 1/F pole and zero proportionately. Therefore, replacing C with a trimmer cap will allow for easy fine-tuning by moving the pole and zero values in tandem while changing the relative position of 1/F zero to the op amp second pole. This will allow the fine-tuning of the phase margin for best results.

Bench Evaluation and Fine Tuning

Design #	C (pF)	R _C (Ω)	R _p (Ω)	Comments
1	100	160	-	R _p negative because R _C is too low
2	47	340	380	
3	27	590	1.36k	
4	10	1.6k	5.4k	



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Here are the actual results of bench testing with the just-derived component values.

As expected, the top waveform highlights that with no compensation, the step response shows ringing and almost 50% overshoot. From the previous slide, Design 2 values (highlighted in the table shown) were then employed with the results showing a reasonably well-behaved step response in the bottom scope photo. The overshoot is measured to be less than 10%. Note that the closest 5% resistor values have been used instead of the exact values in the table.

To explore the effect of reducing the value of C, the center scope photo shows that when this capacitor is reduced to 10 pF, as expected, the overshoot increases and the system will have less than the originally stated goal of 45° phase margin.

Steps to Stabilizing a Closed-Loop Feedback System

- Graphical analysis
- Proper placement of poles and zeros
- Deriving the governing expressions
- Solve for the component values that allow the stability criteria to be met



We were able to analyze and design a stable closed-loop system by employing our knowledge on how the feedback network operates and keeping track of gain and phase around the loop. To do so, we had to use the published data on the active device in the loop, as well as general circuit analysis techniques. The graphical method described was a simplification that allowed insight into the process, which is more than one would get by using computational or hand-calculation analysis.

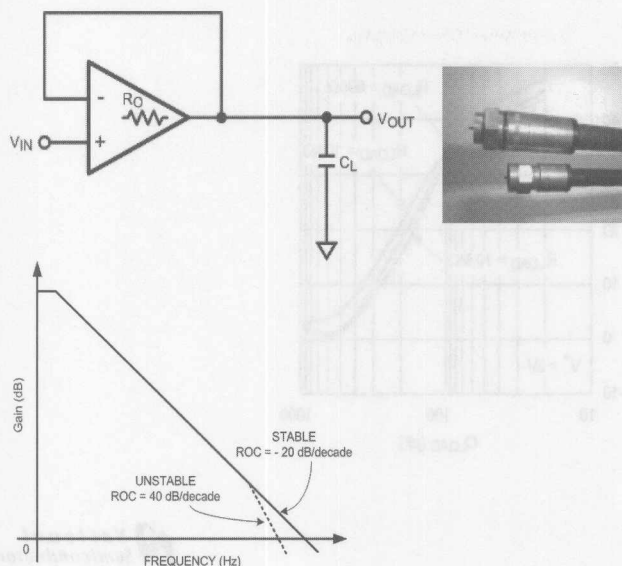
Once the forward- and feedback-path gains are known and plotted, the designer would be in a position to decide on the best placement of the poles and zeroes from the compensation scheme. Having done so, he can put together expressions that define the constraints placed on the pole zero placement. At this point, one can evaluate the component values that meet the criteria. And finally, it is always necessary to evaluate the theoretical calculations by making actual measurements on the bench.

Practical Techniques to Avoid Op Amp Instability Due to Capacitive Loading

We were able to analyze and design a stable closed-loop system by employing our knowledge of how the feedback network operates and looking back of gain and phase around the loop. To do so, we had to use the published data on the active device in the loop, as well as general circuit analysis techniques. The graphical method described was a simplification that allowed insight into the process, which is more than can be gained by using computational or hand-calculation methods.

Once the forward- and feedback-path gains are known and plotted, the designer would be in a position to decide on the best placement of the poles and zeros from the compensation scheme. Having done so, he can put together equations that define the component values on the pole-zero placement. At this point, one can evaluate the component values that meet the criteria. And finally, it is always necessary to evaluate the theoretical calculations by making actual measurements on the bench.

Driving Capacitive Loads



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Capacitive loads are not a matter of choice. In most cases, the load capacitance is not from a capacitor added intentionally, but from things such as PC board traces and coaxial cables. For example, PC board traces have capacitance approximately equal to 22 pF/foot for a 0.025" trace using G-10 dielectric of 0.03" over a ground plane (System Application Guide, Analog Devices, 1993), while a coaxial cable will appear capacitive at the rate of 29 pF/foot for R6-58A/U, a commonly used coaxial cable.

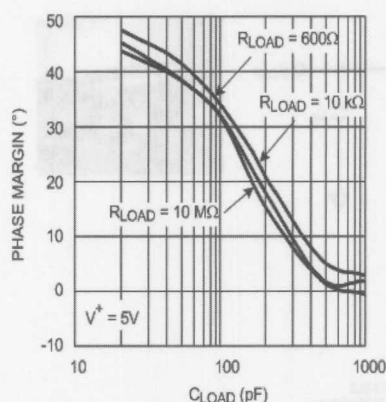
Applications such as sample-and-hold amplifiers and peak detectors require the op amp to drive large capacitive loads, besides the board traces and cables. Some applications may require the amplifier to drive the input of another active device, such as another amplifier or an ADC.

Most op amps are designed to be unity-gain stable for moderate capacitive loads. The amount of capacitive load an amplifier can handle varies. For example, the LM6211 is designed to be unity-gain stable for capacitive load of 100 pF. That is, if connected in a unity-gain, non-inverting buffer configuration, the LM6211 will not oscillate if the capacitive load is 100 pF or less.

Oscillations may occur for higher values of capacitance because amplifiers have an open-loop output resistance R_O . The presence of C_L provides an R_OC_L low-pass filter that introduces phase lag in the output voltage. This increased phase shift reduces the phase margin of a feedback circuit. If there is a significant reduction in phase margin, the transient response will suffer greatly, or the amplifier may be unstable when a large capacitive load is in place.

Amplifiers cannot be designed to be stable for high capacitive loads without either sacrificing bandwidth or supplying higher output stage bias currents. The LM6211 needs to be externally compensated to optimize those applications in which a large capacitive load must be handled at the output of the amplifier.

Amplifier Susceptibility to Capacitive Loads

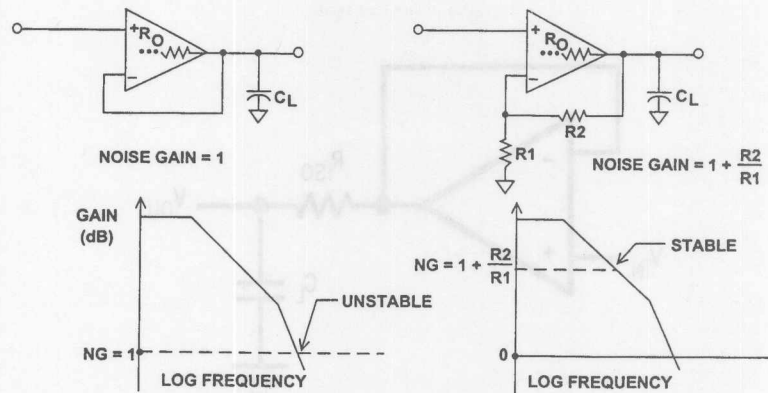


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This graph shows the variation of the phase margin with capacitive load for the LM62111.

The phase margin of an amplifier circuit can be thought of as the amount of additional phase shift at the unity-gain loop frequency of the amplifier required to make the circuit unstable (i.e., phase shift + phase margin = -180°). As the phase margin approaches zero, the loop phase shift approaches -180° and the amplifier circuit approaches instability. Typically, values of phase margin much less than 45° can cause problems such as "peaking" in the frequency response and overshoot or "ringing" in step response. In order to maintain conservative phase margins, the pole generated by capacitive loading should be at least a decade above the circuit's closed-loop, unity-gain bandwidth. When it is not, consider the possibility of instability.

Effects of Capacitive Loading on Amplifiers

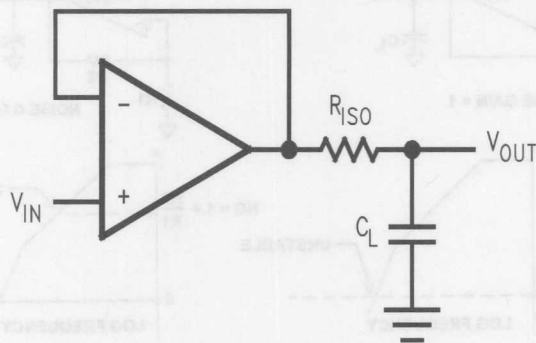


Many designers overlook a powerful way to maintain stability in low-frequency applications which involves increasing the circuit's closed-loop gain (also known as noise gain), thus reducing the frequency at which the product of open-loop gain and feedback attenuation goes to unity.

By increasing the noise gain of the circuit, the unstable situation on the left can be changed to the case on the right, where the intersection of the noise gain plot and open-loop gain happens in the stable region of -20 dB/decade.

Although stability can always be achieved by this method, the bandwidth available to the signal is concomitantly reduced.

Compensating by External Resistor

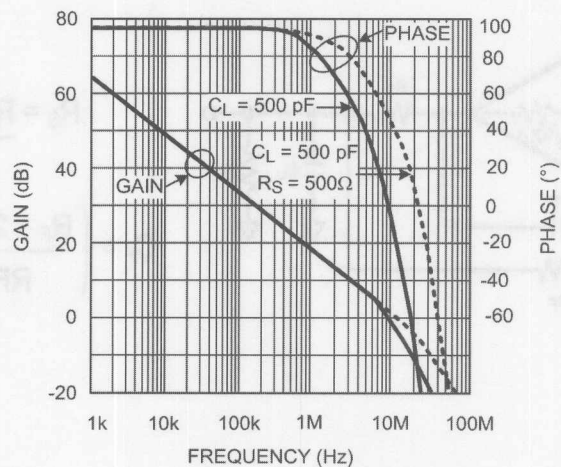


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In some applications, it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. It is possible to use low-phase margin op amps to drive heavy capacitive loads. A simpler scheme for compensation is shown. A resistor, R_{ISO} , is placed in series between the output of the amplifier and the load capacitance. This introduces a zero in the circuit-transfer function, which counteracts the effect of the pole formed by the load capacitance and ensures stability.

The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with lesser ringing and overshoot, but will also limit the output swing and the short-circuit current of the circuit.

Dealing with Load Capacitance (LMV791)

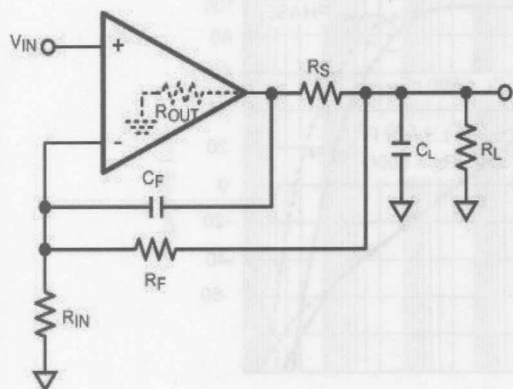


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This graph shows how the isolation resistor can improve the performance of an op amp while driving heavy capacitive load. In this example, the gain and phase margin for the LMV791 was plotted versus frequency. The solid lines show the gain and phase margin of the LMV791 with a capacitive load of 500 pF, which leaves the op amp with zero phase margin, meaning that the device will be unstable. The dotted line shows the plots after inserting an isolation resistor of 500Ω. Adding the isolation resistor restores the phase margin to 40°, and the op amp is again stable.

Min of 40°-60° phase margin possible

In The Loop Compensation



$$R_S = \frac{R_{OUT} R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{R_F^2} \right) C_L R_{OUT}$$

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This circuit illustrates another compensation technique, known as in the loop compensation. This technique employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration.

A small series resistance, R_S , is used to isolate the amplifier output from the load capacitance C_L , and a small capacitance C_F is inserted across the feedback resistor to bypass C_L at higher frequencies. The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L . This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown the values of R_S and C_F are given by equations on the right.

Calculating R_S and C_F (LM6211)

not in 2

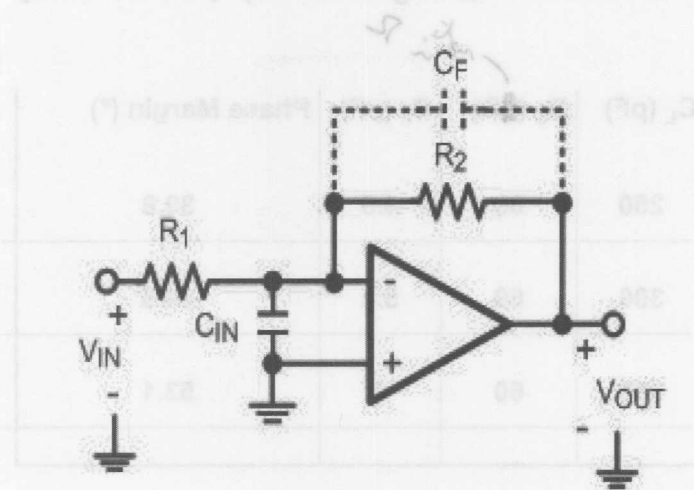
C_L (pF)	R_S (Ω)	C_F (pF)	Phase Margin ($^\circ$)
250	60	4.5	39.8
300	60	5.4	49.5
500	60	9	53.1



Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed-loop bandwidth of the circuit is now limited by R_S and C_F .

This table shows different values of R_S and C_F that need to be used for maintaining stability with different values of C_L , as well as the phase margins to be expected. R_F and R_{IN} are assumed to be 10 k Ω , R_L is taken as 2 k Ω , while R_{OUT} is taken to be 60 Ω .

Stability and Input Capacitance



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In certain applications, such as I-V conversion, transimpedance photodiode amplification, and buffering the output of current-output Digital-to-Analog Converters (DACs), capacitive loading at the input of the amplifier can endanger stability. The capacitance of the source driving the amplifier, the op amp input capacitance, and the parasitic/wiring capacitance contribute to the loading of the input. This capacitance, C_{IN} , interacts with the feedback network to introduce a peaking in the closed-loop gain of the circuit, causing instability.

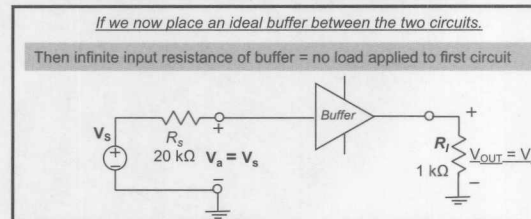
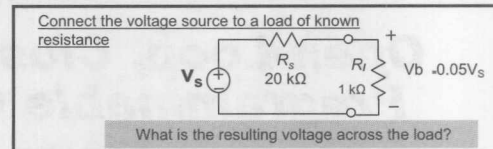
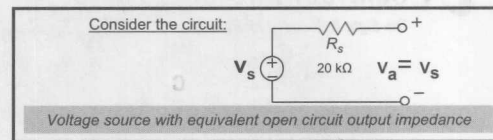
This peaking can be eliminated by adding a feedback capacitance, C_F , as shown. This introduces a zero in the feedback network, and, hence, a pole in the closed loop response, and thus maintains stability. A simple approach is to select $C_F = (R_1/R_2)C_{IN}$ for a 90° phase margin. This approach, however, can limit the bandwidth excessively.

Open-Loop, Closed-Loop, and Programmable Gain Buffers

In this article is a lot of more of the basic and intuitive (non-ideal) buffer rules that help to define a buffer for a given application. Typically, only a few of these parameters are critical for any given application. The buffer can do all of these things well, and trade-offs will always be part of the process. Just said, there is nearly always one rule that is critical to any application where a buffer is used and which really defines what we mean by the term of a buffer. That rule is the ability to buffer a source that is ideal. The measure of how well a given buffer can do this is embodied in its open-loop and output impedance specifications. As can be seen from the (ideal) current specification on the right, a buffer with an input impedance less than infinite would load the source and cause the input signal to not appear at output, while an open-circuit load of more than $10^9 \Omega$ would cause the effective output swing to be less than $V_{cc}/2$ to the load. The ideal buffer for the example above provides a gain of 1 with infinite input resistance (does not require any input current), has zero output resistance (can drive any desired load resistance without loss of signal voltage, output only gain), and therefore, provides a non-inverting, unity-gain buffer. This is the basic rule for the design of a buffer. The design of a buffer is based on the choice of buffer. However, the fact that real buffers don't appear to have infinite input impedance and zero output resistance is not a problem. In fact, many manufacturers represent high-impedance input and low-impedance output as a major feature of their buffers. In fact, many manufacturers represent high-impedance input and low-impedance output as a major feature of their buffers.

Defining a Buffer

- High input impedance
- Unity gain (usually, but not always)
- Low output impedance
- Large current gain
- Large output current drive (usually larger than an op amp's)
- Stable when driving large and varying capacitive loads
- High speed/wide bandwidth
- Low operating current
- Low noise
- Low distortion



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In this slide is a list of some of the desirable, and attainable (non-ideal), buffer traits that help to define a buffer for a given application. Usually, only a few of these parameters are critical for any given application. No buffer can do all of these things well, and trade-offs will always be part of the process. That said, there is nearly always one trait that is critical in any application where a buffer is used and which really defines what we mean by the idea of a buffer. That trait is the ability to isolate a source from a load. The measure of how well a given buffer can do this is embodied in its input impedance and output impedance specifications. As can be seen from the (ideal) circuit specification on the right, a buffer with an input impedance less than infinite would load the source and attenuate the input signal to one degree or another, while an output resistance of more than 0Ω would reduce the effective output swing, thus providing less than V_s to the load. The ideal buffer for the example above provides a gain of 1 with infinite input resistance (does not require any input current), has zero output resistance (can drive any desired load resistance without loss of signal voltage, ergo unity gain), and therefore, provides a tremendous impedance-level transformation while maintaining the level of the signal voltage. How far the results are from these ideals will depend upon the application and the choice of buffers. However, the fact that real buffers don't approach these ideals makes them no less useful.

Because many transducers represent high-source impedance, a unity-gain buffer is found in many sensor and data-acquisition applications.

When to Use a Buffer

- **For an impedance transformation from a high impedance source to a low impedance load, such as driving a coaxial cable (Matching)**
- **To minimize the influence on a signal source (oscillator, sensor, sample and hold, filter, etc.), of a varying load impedance such as that found at the inputs of $\Delta\Sigma$ and flash ADCs (Isolation)**
- **To boost the drive capability of an op amp or other device (Current Gain)**
- **To distribute stable, clean signals through transmission lines or on PC boards or to external equipment (Matching, Isolation, Current Gain)**



For a case where a signal source does not have a low enough output impedance to drive a load, one can increase the output drive capability by using a buffer. For example, an oscillator might experience an unacceptably high frequency shift or stop working altogether when loaded heavily. A buffer is called for in that situation so as to isolate the load from the oscillator.

Buffers are very often used to drive (match) passive loads, such as terminated and unterminated coaxial cables, as well as the metal traces (e.g., strip lines) on PC boards. But they also are called upon to drive the signal inputs to other active devices (matching, isolation), such as ADCs. The inputs to many ADCs represent a very large and varying reactive load at their input terminals. For example, a flash ADC presents a large and non-linear capacitive load that is very signal dependent. A buffer with a low output impedance and the ability to remain frequency stability while driving a nanofarad or more is needed here. Pipelined ADCs also present a difficult challenge to a buffer. These ADCs consist of differential inputs into an analog switch, followed by a switched capacitor amplifier, and sample and hold. Besides seeing a purely capacitive input impedance that changes with each clock cycle, the external input buffer must deal with large voltage spikes that are caused by the large current pulses that occur when the internal sampling switch opens and closes. The buffer must be able to absorb these spikes without distorting the signal.

There are times when it is desirable to provide an op amp with more output drive (current gain) than it can supply by itself. Any buffer can be put inside an op amp feedback loop. In this case, the buffer solves the load drive problems, while the op amp maintains the low signal level precision required. The op amp also can provide additional gain to the overall circuit. In addition, the op amp is not affected by the heat dissipated in the buffer when driving heavy loads, and thus does not experience any unwelcome thermal feedback problems. However, when an op amp is placed inside the buffer/op amp loop, an additional phase lag, introduced by the buffer, must be included in loop stability considerations.

Classes of “Dedicated” Buffers

Open Loop:

- Wider C_L range capability**
- Fast slew rate/wide bandwidth**
- High output current drive**
- Simpler/less expensive**
- Shorter propagation delay**

Closed Loop:

- Fast slew rate/wide bandwidth**
- Lower distortion**
- Lower gain error/linearity**
- Better DC specs (V_{OFFSET} , R_{OUT})**
- High output current drive**



By “dedicated,” we mean amplifiers that are not a modified “something else.” For example, they are not op amps configured in a gain of 1 (this is possible, and is done, but can be expensive and/or non-ideal for the task). But, by and large, unmodified op amps don’t have the special combination of qualities that make the best buffers. Dedicated buffers are components that are designed expressly to isolate source and load.

Buffers have been around for many years in integrated circuit form, ever since National Semiconductor introduced the LH0002 many years ago. They can be divided into two broad classes: Open loop and closed loop. As a decision problem facing the designer, sorting out which class to use in a given application can sometimes be confusing. Tradeoffs are inevitable.

To begin with, a closed-loop buffer is essentially an op amp that has been optimized for unity-gain operation. Since it is internally compensated for unity-gain stability, it will, as a class, be inherently slower than the open-loop variety (although exceptions abound). However, it will generally have more accurate DC characteristics, display lower distortion, and have better gain linearity. Still, the open-loop approach commonly allows for wider bandwidth, shorter propagation delay, and greater stability over a wider range of capacitive loads. Also, their simpler circuit topologies (basically they are glorified complementary emitter followers) make open-loop buffers a cheaper alternative. Still, when it comes right down to it, the objectives of the application circuit will dictate which type to go with.

If our buffer were perfect, it would display zero output impedance at all frequencies of interest, infinite input impedance (0 input current), infinite bandwidth and slew rate, and a voltage gain of precisely 1 (output = input). Failing to attain those lofty goals, to one degree or another, we will settle for a buffer that has a measurably insignificant effect on the fidelity of the signal and gets along with its fellows (doesn’t load its sources while presenting an essentially low-impedance voltage source to the load).

A Buffer for Most Occasions

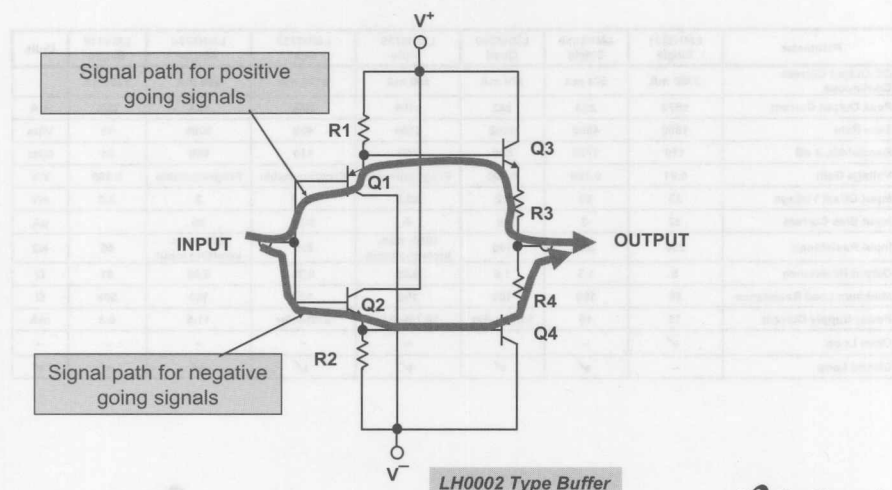
Parameter	LMH6321 Single	LMH6559 Single	LMH6560 Quad	LMH6739 Triple	LMH6718 Dual	LMH6704 Single	LMV115 Single	Units
DC Output Current Continuous	±300 mA	±74 mA	±74 mA	±90 mA	±170 mA	±90 mA	±205 μ A	
Peak Output Current	±570	±83	±83	±160	N/A	N/A	N/A	mA
Slew Rate	1800	4580	3100	3300	400	3000	18	V/ μ s
Bandwidth, 3 dB	110	1750	680	750	110	650	31	MHz
Voltage Gain	0.91	0.996	0.995	Programmable	Programmable	Programmable	0.998	V/V
Input Offset Voltage	±3	±3	±2	±0.5	±0.6	2	3.5	mV
Input Bias Current	±2	-3	-5	-8	±0.6	±5		μ A
Input Resistance	250	200	100	1000; non- inverting input	380	1000; non- inverting input	65	k Ω
Output Resistance	5	1.3	1.6	0.05	0.28	0.05	61	Ω
Minimum Load Resistance	50	100	100	100	100	100	50k	Ω
Power Supply Current	15	10	11.5/buffer	10.7/buffer	2.4/buffer	11.5	0.3	mA
Open Loop	✓	-	-	-	-	-	-	-
Closed Loop	-	✓	✓	✓	✓	✓	✓	✓



The characteristics of a selection of National's buffers are summarized and contrasted in the table above. While these particular tests can be considered relevant to buffers in general, only a few will be considered critical for a given application. The suitability of a particular buffer is usually determined by, at most, three or four key specifications, and perhaps one or two 'would love' capabilities as well. For example, the demands on a coaxial cable driver become more severe the faster the signal becomes. Thus the most vital considerations for the buffer would probably be output current drive, slew rate, and bandwidth capabilities. These are common requirements for all such applications. However, in a field of several competing buffers, where all adequately meet these requirements, the best choice might be the one that has the lowest THD + N or the best gain flatness. Some buffers that are designed for specific markets have been optimized for certain key parameters of that market. For example, the LMH6739 specifies differential gain and differential phase, two parameters that have not commonly been specified by buffers, but which nevertheless are of paramount importance in analog video systems, where this buffer finds use. While most of the buffers presented here are intended for use alone, or in a closed-loop combination with op amps to drive coaxial cables and capacitive or other moderate to high-current loads, the one exception is the LMV115. This buffer is specially designed as an oscillator buffer to reduce the effects of spurious signals from the baseband chip to oscillator (in such portable applications as cellular phone, GSM modules, and oscillator modules) and to isolate the oscillator from the effects of varying load capacitance and resistance. In these portable applications, low supply current is more important than speed or output current.

Although the term buffer is largely accepted to mean a device that supplies current gain but no voltage gain, some applications require that the buffer allow for some voltage gain adjustment (e.g., -1 to +2) while still performing the essential function of isolation. Three of the buffers (LMH6739; LMH6718; LMH6704) have this gain feature. The rest are configured internally to provide a gain of one.

"Classical" Open-Loop Buffer Architecture



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The circuit shown above is the classical embodiment of the open-loop buffer, as first developed in the prior industry standard, the LH0002. Therefore, the LH0002 is a good starting place for which to understand this class of buffer. The input stage consists of complementary bipolar emitter-followers, Q1 and Q2. The symmetrical class AB amplifier output transistors, Q3 and Q4, provide current sourcing or sinking and a relatively constant low impedance to the load. Q1 and Q3, along with Q2 and Q4, make up symmetrical compound emitter-followers with a small-signal current gain of approximately 40,000 (product of first and second stage betas). This combination of cascaded emitter-followers will produce close to unity-voltage gain.

Input stage operating current is determined by R1 in conjunction with supply and input voltages. The emitter-base junction of the first and second stages appear in series between input and output terminals, therefore the output offset voltage for $V_{IN} = 0$ is the difference in base-emitter junction voltages of the PNP and the NPN transistor. This is true for both upper and lower halves of the circuit, so there is no conflict between the two circuit halves. Output stage quiescent current will equal that of the input stage if the transistors are matched and at equal temperatures. This establishes a class AB bias in the output stage so there is no class B crossover distortion in the output. Resistors R3 and R4 inserted in the output emitter circuits minimize the effect of unmatched upper and lower circuit halves and limit the potential for thermal runaway due to input and output stage temperature differences.

“Classical” Open-Loop Buffer Architecture

Operation is symmetrical. Analysis can be carried out using a half circuit

For the basic circuit the operating current is determined by R1 in conjunction with supply and input voltages

$$I_C = \frac{V_S - V_{BE} - V_{IN}}{R1} \quad (1)$$

Maximum output current is dependent on the supply voltage, R1, Q3 current gain, and the output voltage

$$I_{O(MAX)} = \frac{V_S - V_{BE3} - I_O R3 - V_O}{R1 / \beta^3} \quad (2)$$

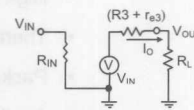
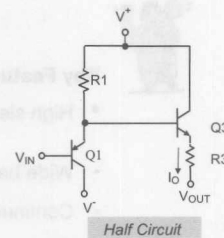
$$= \frac{V_S - V_{BE3}}{R1 / \beta^3 + R3 + R_L} \quad \text{where } \beta^3 \approx 200$$

Gain expression written as a function of load resistance and input voltage is:

$$A_v \equiv \frac{R_L}{R_L + R3 + r_{e3}} = \frac{R_L}{R3 + R_L \left(1 + \frac{0.026}{V_{IN}} \right)} \quad V_{IN} > 0.1V \quad (3)$$

where $r_{e3} = \frac{V_T}{I_O}$, and $\beta^3 \approx 200$

note that 0.026V = thermal voltage, V_T , at 25°C



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Maximum output current is dependent on the supply voltage, R1, Q3 beta, and the output voltage. Maximum current is available when V_{IN} rises sufficiently above V_{OUT} that Q1 is cut off. Under this condition, R1 supplies base current to Q3, and maximum output current is given by Equation 2.

The voltage gain is slightly less than unity and is a function of load. It is dominated by the finite output resistance of the output stage. Hence, the gain analysis can utilize the hybrid model. Note that r_{e3} is the emitter dynamic resistance of Q3 and is load-current dependent. The gain expression written as a function of load resistance and input voltage is shown in Equation 3.

When it was introduced, the LH0002 represented a quantum step in IC buffer design. However, it had two major compromises in its design. The first compromise can be understood by referring back to the previous slide.

Compromise 1: Transistors Q3 and Q4 are made relatively large to provide the desired output current. Thus, the major frequency limitation is present at the bases of these transistors (collector-base capacitances of Q1 – Q4). Q3 and Q4 are turned on by the current flowing in resistors R1 and R2, respectively. Since the resistance values are established by the quiescent operating current (they are typically about 5 kΩ), they will limit the turn-on current to the output transistors. Turn on would be improved if these resistors were made smaller, but this would increase quiescent current and input bias current. Thus a speed/power trade-off is created.

Compromise 2: In terms of small signal behavior, the LH0002 could typically attain small signal bandwidths of about 30 MHz when using a 50Ω load and a 100 mV signal. This was possible because the LH0002 used hybrid (discrete transistor) construction. The PNP transistors used in monolithic integrated circuits have poor high-frequency performance relative to the NPNs, because of longer base transit times and lower carrier mobility. Thus discrete, vertical PNP transistors were used.

The LMH6321: An Improved High-Speed, Open-Loop Buffer



Key Features (Typical values)

- High slew rate -1800 V/μs into 50Ω
-2900 V/μs into 1 kΩ
- Wide bandwidth: 100 MHz
- Continuous output current: ±300 mA
- Wide supply voltage range: 5V to ±15V
- Programmable current limit
- High capacitive load drive
- Thermal shutdown error flag
- Packages: PSOP-8 and TO263-7
- Applications: line driver, pin driver, sonar driver, high density buffering



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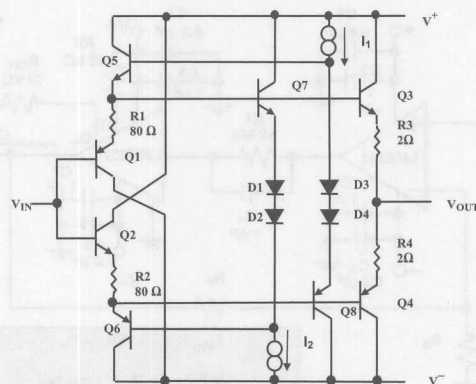
New buffer: It was desirable to manufacture a fully monolithic version of such a buffer, but with none of the previously mentioned compromises. It would be possible to eliminate Compromise 2 provided a suitable monolithic PNP device were developed and Compromise 1 eliminated with design enhancements. With the development of National's patented Vertically Integrated PNP (VIP) process, a new, improved version of the venerable LH0002 was created. The VIP process, which includes trench isolation rather than junction isolation, allowed for the creation of complementary NPN and PNP transistors on the same die with greatly improved transition frequency (F_T) performance. This new buffer is called the LMH6321 (simplified diagram shown above), with the H in the prefix standing for high speed. The LMH6321 has performance of

- >100 MHz GBW
- 300 mA continuous output current drive capability, 700 mA peak
- Slew rate = 1800 V/μs into a 50Ω load

In addition, the LMH6321

- is stable driving any capacitive load
- allows for external programming of maximum output current with just one resistor
- comes equipped with an error flag
- has on-chip thermal shutdown in the event of a sustained short circuit to ground

The LMH6321: An Improved High-Speed, Open-Loop Buffer



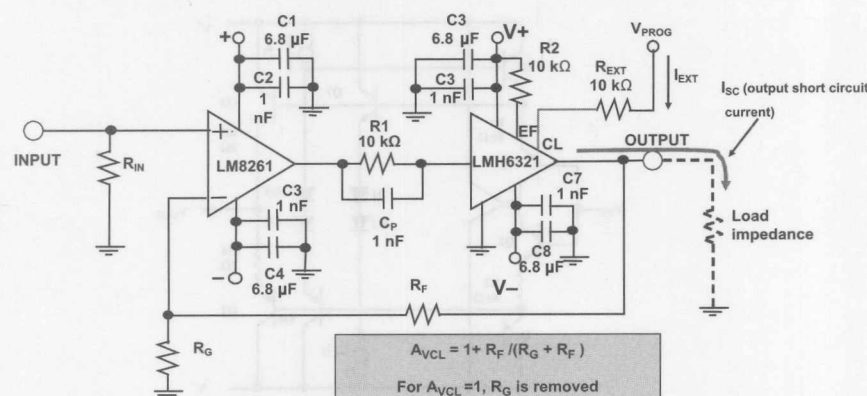
Simplified schematic of core buffer



The input to the driver stage includes active-load devices cross-coupled to the output stage inputs so that the output stage is bootstrap driven from emitter followers. The circuit is biased by level shifting means (I_1 , I_2 , D1 – D4) to operate as a class AB current amplifier. Each of the bases of the output transistors is returned to its collector supply by way of an active load transistor (Q5, Q6) that is connected as an emitter-follower to drive the opposite half of the circuit. Thus, the active load devices have their inputs cross-coupled to the input transistors and effectively bootstrap the output transistor drive. This means that the output transistor base capacitances are both charged and discharged through active transistors, and the circuit is thereby sped up in its signal drive operation. Complementary transistors Q5 and Q6 are connected as the active loads for transistors Q1 and Q2, respectively. They are connected as emitter-followers that are bootstrap-driven by cross-coupling from the complementary or mirror image of the circuit. Resistors R1 and R2 have low values selected to determine the circuit quiescent current and improve stability with capacitive loads. Each of the bases of the output transistors (Q3 and Q4) is charged and discharged by means of an active transistor that quiescently carries much less current than the amount needed to drive the output transistors quickly on and off under conditions of output loading. Thus, the compromises required in the LH0002 are avoided.

When more output current is required from an op amp, a wide band unity-gain buffer can be included in the feedback loop. This has the added feature of improving an open-loop buffer's DC performance (i.e. gain linearity, gain error, offset, output impedance, etc.) due to the very large loop-gain of the combination. In addition, the op amp is not affected by the heat dissipated in the buffer while driving heavy loads, and thus does not suffer the negative effects of thermal gradients on its low-level input stage. However, adding a buffer to the feedback loop will add another pole (phase lag) to the response. If the unity-gain crossing of an op amp is near the GBW of the buffer, the over all phase lag of the circuit will consume most, if not all, of the available phase margin, and oscillation will occur. For this reason, it is important to use a buffer with a GBW significantly larger than that of the op amp, so that loop performance will be determined solely by the op amp.

Buffered Op Amp Loop Using the LMH6321



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Compared to most general-purpose, precision, and low-power op amps, the bandwidth of these buffers is so great that the op amp totally controls the loop stability. If a wideband op amp is used, the phase margin and open-loop frequency response can be altered by the additional pole(s) contributed by the buffers, and this should be taken into consideration. The buffer phase shift is algebraically summed with the op amp phase shift and may cause a stable op amp loop to become marginally stable (large overshoot, ringing), depending on the relative positions of the op amp and buffer poles. In the application above, the LM8261 op amp has a GBW of 15 MHz, while the -3 dB bandwidth of the LMH6321 is greater than 100 MHz.

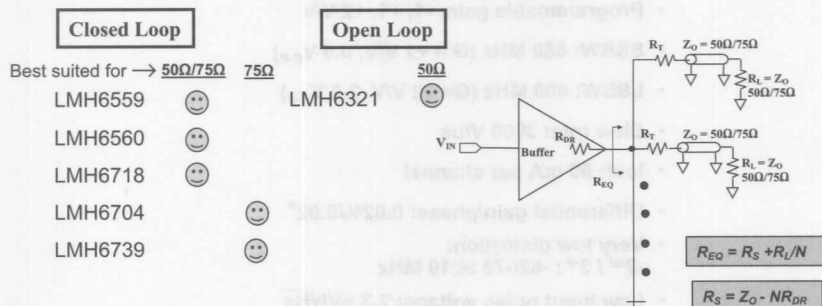
The LMH6321 buffer has two features not found in most buffers of its class, namely a programmable output current and an Error Flag (EF) pin. The LMH6321 provides an open collector output at the EF pin that produces a low voltage when the thermal shutdown protection is engaged due to a fault condition. Under normal operation, the EF pin is pulled up to $V+$ by an external resistor. When a fault occurs, the EF pin drops to a low voltage and then returns to $V+$ when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. Thermal shutdown can occur due either to improperly heat sinking the buffer or from an extended short circuit condition, or both. The output current can be programmed by a single external resistor and voltage source for up to 300 mA of continuous current. This current is accurate to $5 \text{ mA} \pm 5\%$. The value of the resistor for any program voltage and output current I_{SC} is

$$R_{EXT} = 400V_{PROG}/I_{SC}$$

Keep in mind that the LMH6321, like all high-current buffers, must be attached to a heat sink when driving heavy loads that can push the junction temperature above the operating range of the device. The datasheet for this part gives detailed advice on how to do this by using the copper area of the PC board as a heat sink. Resistor R_1 is recommended as a protection for the input stage of the LMH6321 in the event of an input/output differential voltage of greater than 5V. This can happen with an output short to ground while driving the inputs to $\pm 15\text{V}$. Capacitor C_1 is a feed-forward cap to compensate for the pole created by the buffer's input resistance and capacitance. Thus C_1 is given by

$$C_1 = 5(R_{IN})/(R_1)(3.5 \text{ pF}), \text{ where } R_{IN} = 250 \text{ k}\Omega$$

Cable Distribution Driver



Cable/Transmission Line Distribution

The 75Ω termination implies an RGB video distribution system



When driving multiple transmission lines, the load presented to the driver is R_{EQ} , above, where (assuming all transmission lines have the same impedance):

R_{EQ} = equivalent load seen by the line drive R_S = source terminating resistance
 R_L = load terminating resistance N = number of transmission lines

The buffers suggested here are single, dual, triple, and quad devices capable of delivering 74 mA to 300 mA continuous and 83 mA to 570 mA peak output current per driver.

Do not ignore the output impedance of the buffer/drivers, even though this impedance is usually very low. Even in a closed-loop buffer, the output impedance may be significant at high frequencies, where it tends to increase. The value of the source resistor should follow this equation:

$$R_S = Z_O - (N)(R_{DR})$$

R_S = Source termination resistor value Z_O = Characteristic line impedance
 R_{DR} = Effective output resistance of line driver at frequency N = Number of driven lines

Without this consideration, any reflections on one transmission line will effect what is happening on the other lines. That is, if the load termination resistors are not optimum, the reflections back to the line driver from one line may couple into the other lines. If the timing of the reflections are different, signal integrity could be compromised.

The problem here might be in the dividing of the signal. This can be compensated for by increasing the gain of the buffers that are gain-programmable. This may not be easy, but it is possible for unity-gain buffers by putting them into an op amp feedback loop and adding the necessary gain.

LMH6704: Single, Programmable Gain Buffer

- Programmable gain: -1, +1, +2 V/V
- SSBW: 650 MHz ($G = +1$ V/V, $0.5 V_{p,p}$)
- LSBW: 400 MHz ($G = +2$ V/V, $2.0 V_{p,p}$)
- Slew rate: 3000 V/us
- Iout: 90 mA per channel
- Differential gain/phase: 0.02%/0.02°
- Very low distortion:
-2nd / 3rd: -62/-78 at 10 MHz
- Low input noise voltage: 2.3 nV/√Hz
- Disable
- SOT23-6 and SOIC-8 packages
- Pin compatible to OPA692
- Replacement for HFA1112



The LMH6704 is a current-feedback Programmable Gate Array (PGA) and has been designed to provide excellent performance with production-quality video signal in a wide variety of formats such as HDTV and high resolution VGA. NTSC and PAL performance is nearly flawless with differential gain of 0.02% and differential phase of 0.02°. Most professional video processing amplifiers/buffers require differential gain and phase to be less than 0.1% and 0.1°, respectively.

$$R_{in} = R_{out} - (R_{in} + R_{out})$$

$$R_{in} = \text{Characteristic line impedance}$$

$$R_{out} = \text{Source termination resistor value}$$

$$R_{in} = \text{Effective input impedance of the driver at frequency } f = \text{Number of driver lines}$$

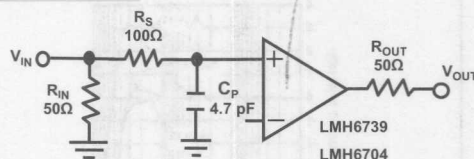
Without the termination any reflections on the transmission line will affect what is happening on the other line. That is, if the load termination resistor is not present, the reflections back to the bus drive from one line couple into the other line. If the timing of the reflections are different, signal integrity could be compromised.

The problem here might be in the dividing of the signal. This can be compensated for by increasing the gain of the buffers that are gain-programmable. This may not be easy, but it is possible for unity-gain buffers by putting them into an op-amp feedback loop and adding the necessary gain.

Programmable Gain Buffer

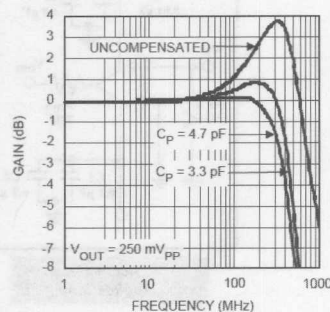
Buffer gain is set to $A_V = +1$, which is worst case for peaking

•Correct for Unity Gain Peaking



INPUT CONNECTIONS		
Gain A_V	Non-Inverting (Pin 3)	Inverting (Pin 4)
-1V/V	Ground	Input Signal
+1V/V	Input Signal	NC (Open)
+2V/V	Input Signal	Ground

GAIN CHART

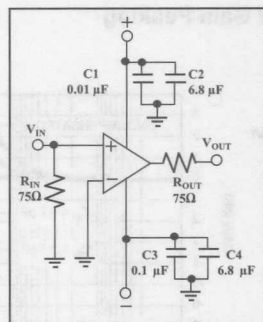


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The LMH6739 and LMH6704 are Programmable Gain Buffers (PGBs) that are very useful in high-speed video applications. They essentially are very high-speed, closed-loop current feedback op amps. Their gain setting resistors, the feedback resistor (R_F) and input resistor (R_G) are built on the chip. $R_F = R_G = 450\Omega$, for the LMH6739 and 465Ω for the LMH6704. Thus, they can be configured with $A_V = +2$, $A_V = +1$, or an $A_V = -1$ by connecting pins 3 and 4 as noted in the chart. The gain accuracy for these buffers is accurate and guaranteed over temperature to within $\pm 1\%$. The internal gain-setting resistors match very well. The buffers' architecture takes advantage of the fact that these resistors track each other very well over a wide range of temperatures and process variation to keep the overall gain constant, despite the fact that the individual resistors have nominal temperature drifts. Therefore, it is not recommended that external resistors be put in series with R_G to change the gain, as this can result in poor gain accuracy over temperature.

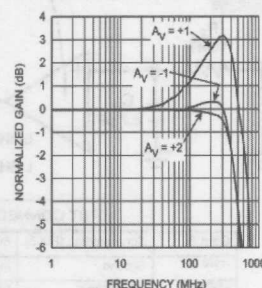
With PGBs that use current-feedback architecture, like the LMH6739 and the LMH6704 as well as the LMH6718, the feedback resistor, R_F , is a compromise between the value needed for stability at unity gain and the optimized value used at a gain of +2. The result of this compromise is substantial peaking in some cases at unity gain, as you can see here. If this peaking is undesirable, a simple RC filter at the input of the buffer will smooth the frequency as shown. The graph to the left shows the results of a simple filter placed on the non-inverting input in the schematic.

LMH6704: Single, Programmable Gain Buffer



Typical Video
Application

Small Signal Frequency Response vs. Gain

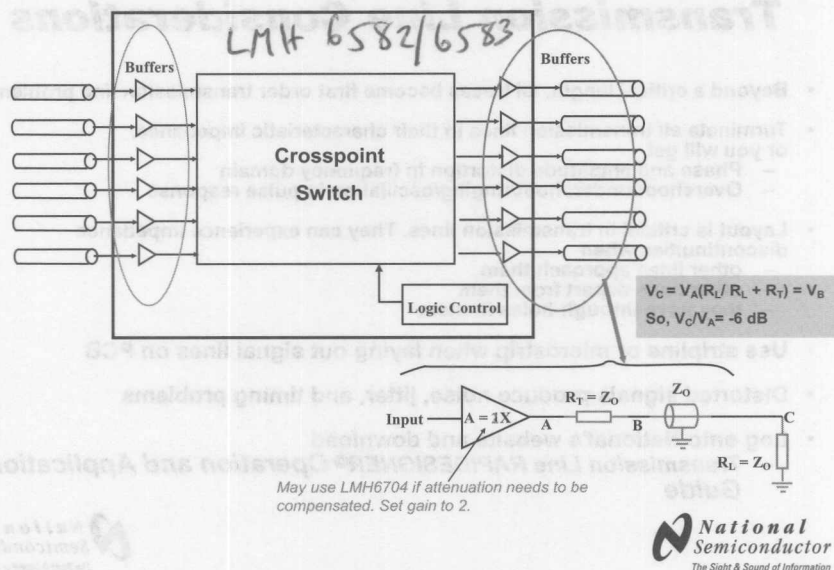


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Best performance is obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

With the inverting pin grounded, as shown in the typical application circuit, the gain of the buffer is +2. This accomplishes two things. First, it compensates for the loss of -6 dB caused by using back termination, and second, it flattens the gain vs frequency characteristics near the roll-over frequency, as shown in the frequency response curves.

Simplified Buffer Application for Analog Router/Switcher



The slide shows a typical application for input and output buffering for routing and switching platforms. Here, un-buffered input/output analog crosspoint switches are buffered by such suitable devices as National's LMH6704 or LMH6559. These are single devices. Note that we did not include the quad LMH6560 or the triple LMH6739, although they could also be used because many designers prefer single buffers in order to minimize crosstalk in the system.

A simplified diagram for the output buffer circuit is shown in the bottom-right of the slide. Note that a resistance, R_T , has been placed in series between the output of the buffer and the transmission line. This back-termination, while not always needed, ensures that the input to the transmission line will be properly loaded with its characteristic impedance in order to eliminate the possibility of reflections. However, this will reduce the signal level at the load end by 6 dB. If this loss is unacceptable, then it is recommended that the LMH6704 be used and the gain set to 2x to compensate for the loss.

Maintaining Signal Integrity When Using High-Frequency Buffers: Some Transmission Line Considerations

- Beyond a critical length, all traces become first order transmission line problems
- Terminate all transmission lines in their characteristic impedance, or you will get
 - Phase and amplitude distortion in frequency domain
 - Overshoot/undershoot/ringing/oscillation in pulse response
- Layout is critical in transmission lines. They can experience impedance discontinuities when
 - other lines approach them
 - other lines depart from them
 - they have through-holes in them
- Use stripline or microstrip when laying out signal lines on PCB
- Distorted signals produce noise, jitter, and timing problems
- Log onto National's website and download
 - *Transmission Line RAPIDESIGNER® Operation and Application Guide*



With op amp and buffer bandwidths already in the hundreds of MHz and some pushing well into the GHz region, it is imperative that attention focus more and more on the parasitic-rich neighborhoods in which these devices find themselves. Neglecting the effect of parasitic capacitance and inductance on signal integrity is a sure way to compromise the performance of the application.

Too frequently the designer makes simplified and un-justified assumptions, i.e., is the load resistive or is it capacitive? Further, there is no such thing as a purely capacitive load, or even one that is only resistive. As the wavelength of the signal gets shorter, a point is reached where the line is crossed from lumped circuit components to distributed components. At this point, metal trace interconnects and other signal carrying lines become transmission lines. The reason for this is that at sufficiently high frequencies, all of the parasitic 3rd and 4th order components associated with these lines—series inductance, parallel capacitances, equivalent resistances suddenly become first order terms.

All transmission lines must be properly terminated in their characteristic impedance or the signal source will see a wildly varying impedance and phase at the higher frequencies. This will cause reflections of some of the frequencies making up the signal and cause distortion. An un-terminated line can look either capacitive or inductive, depending on the length of the line and the frequency. The input impedance Z_{IN} of a transmission line with a characteristic impedance Z_O and length L , terminated in a load Z_L is given by:

$$Z_{IN} = Z_O \frac{Z_L + jZ_O \tan \beta L}{Z_O + jZ_L \tan \beta L}$$

Where $\beta = 2\pi/\lambda$, and λ is the size of one wavelength on the line. The output impedance of a driver is significant in two ways. First, it is of interest in terms of how it matches the Z_O of the transmission line it is connected to. Second, it is of interest when understanding what the magnitude of the wave it launches down the transmission line will be. If, for example, the transmission line is a standard RG58C/U coaxial cable and we terminate the line in 50Ω , then by the above equation $Z_{IN} = Z_O$ and the cable will look like a pure 50Ω resistance over frequency. Assuming both ends of the cable are terminated thus, then there should be no reflections and no distortion. Half of the signal power will have been absorbed by the load impedance and half by the source impedance.

PCBs should use stripline or microstrip geometries for signal distribution at very high frequencies. A good place to find a practical and simple guide to do this is on National's website. Here one can download the Transmission Line RAPIDESIGNER Operation and Applications Guide, for a step-by-step aid to designing fool-proof board transmission lines.

When is Termination Needed?

- Transmission lines should be terminated
- Simple traces need not be terminated
- Trace becomes a transmission line at:

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}}$$

Where t_r is the digital signal rise time
 t_{PR} is the signal propagation rate

Typical t_{PR} is about 150 ps/inch on board of
FR-4 material



Sometimes we can get away with treating a signal line as a simple trace. However, this begs the question, "When must a trace be considered a transmission line?" The formula in the slide tells us that the line length beyond which a trace must be treated as a transmission line is a function of the signal rise time and the propagation rate of the signal across the board (a function of board material). When in doubt, always treat the line as a transmission line.

For analog signals, the rise time can be approximated by treating the signal as if it were a trapezoid with edge rates equal to the maximum slew rate of the signal. For monotonic sine waves, the rise time is about 30% of the sine wave period.

Question: Is Termination Needed?

?

The LMH6559 has an output signal rise time of 0.4 ns. The PCB is a typical one of FR-4 material. Beyond what line length should the line be properly terminated?

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}} = \frac{0.4 \times 10^{-9}}{6 \times 150 \times 10^{-12} \text{s/in}}$$

$$\text{Maximum Length} = \frac{10^3}{2250} = \underline{0.44 \text{ inches}}$$

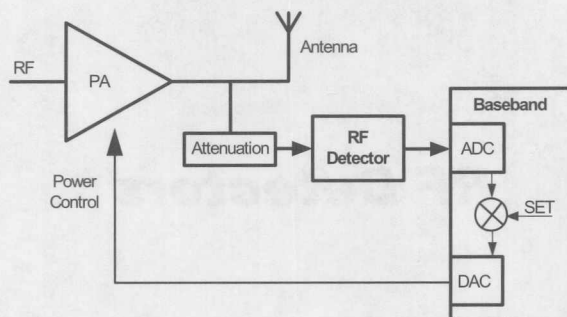


As a practical example, let's look at the case of a very fast buffer—in this instance the LMH6559. This buffer has a published rise time of 400 ps. So, if we want to know what the maximum allowed signal trace length would be before termination is required, we just plug this rise time into the previous equation, and discover that less than half an inch of un-terminated line is allowed. Beyond this length, transmission line effects start to dominate, and we need to terminate the line. One should subtract about 10% from the calculated length for safety.

RF Detectors

In a cell phone it is important to set the output level of the Power Amplifier (PA) precisely. This is necessary to transmit the correct power level, which is dictated by the base station, and to compensate for local temperature and other variables that can affect the output power of the PA. A well-established method to set the power level precisely is to use closed-loop power control. The RF detector measures the PA output power through an attenuator and the measurement is compared with the desired level to the feedback signal processing unit. A DAC applies a control signal to the PA in order to set the correct level. CDMA and WCDMA are examples of applications where such a closed-loop power control can be used. The response time of the control loop in these applications doesn't have to be very fast, as opposed to GSM (TDMA), and this allows implementation of the control scheme in the feedback chip.

General Block Diagram



The RF detector measures output power and controls the PA's output to set the desired power level



In a cell phone it is important to set the output level of the Power Amplifier (PA) precisely. This is necessary to transmit the correct power level, which is dictated by the base station, and to compensate for local temperature and other variables that can affect the output power of the PA. A well-established method to set the power level precisely is to use closed-loop power control. The RF detector measures the PA output power through an attenuator and that measurement is compared with the desired level in the baseband signal processing unit. A DAC applies a control signal to the PA in order to set the correct level. CDMA and WCDMA are examples of applications where such a closed-loop power control can be used. The response time of the control loop in these applications doesn't have to be very fast, as opposed to GSM (TDMA), and this allows implementation of the control scheme in the baseband chip.

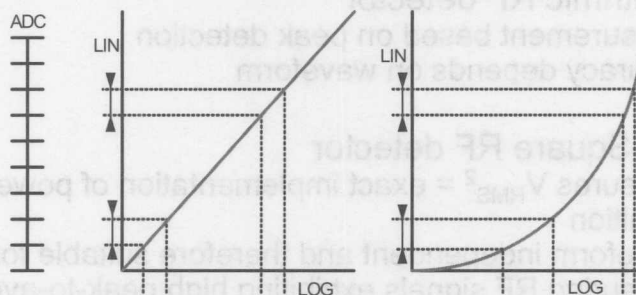
RF Detector Types

- Logarithmic RF detector
 - Measurement based on peak detection
 - Accuracy depends on waveform
- Mean-Square RF detector
 - Measures V_{RMS}^2 = exact implementation of power definition
 - Waveform independent and therefore suitable for measuring RF signals exhibiting high peak-to-average ratios used in 3G and UMTS/CDMA applications



National offers both logarithmic and mean-square detectors as well as power amplifiers. Logarithmic detectors are based on peak detection, V_{PEAK} , while a mean-square detector measures V_{RMS}^2 . Peak detection is less accurate for power-level detection because the relation between peak voltage and average power depends on the waveform. For a steady state sine wave of V_{PEAK} volts across a 1Ω load, the average power is $(V_{\text{PEAK}})^2/2$ Watts. A triangular wave form with the same peak amplitude across the same load will deliver an average power of $(V_{\text{PEAK}})^2/3$ Watts. With more complex waveforms, such as the CDMA signal, the measurement error can be in the order of 5 to 6 dB. Therefore, for many wave forms, especially those with high peak-to-average ratios, peak detection may not be accurate enough. A mean-square detector would be recommended. On the other hand, when the log detector signal is processed through a linear input ADC to provide the PA control voltage, the log detector will provide equal resolution over the power range. A square law detector will have more resolution at higher power levels than at low power levels.

Measurement Resolution



Logarithmic detector:
Constant resolution over
entire range

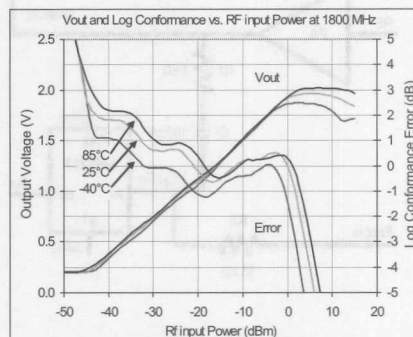
Mean-Square detector:
Reduced resolution in low
power range

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Many baseband signal-processing chips have ADCs with limited resolution, for instance 8-bit or 256 steps. These steps are linearly divided over the converter input-voltage range. It can be seen that the logarithmic detector has constant resolution over the complete power range, making a logarithmic transfer preferred. Mean-square detectors with a log-log response have more limited resolution at lower power levels, as can be seen on the right-hand side. Therefore, mean-square detectors are normally used in the steep part of the curve.

Logarithmic Detector

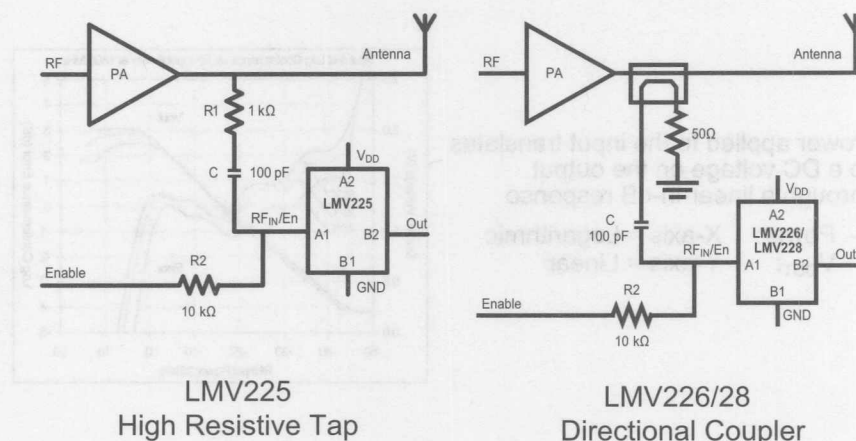
- Power applied to the input translates to a DC voltage on the output through a linear-in-dB response
 - Power: X-axis = Logarithmic
 - V_{OUT} : Y-axis = Linear



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Power applied to the input of a logarithmic detector translates to a DC voltage on the output through a linear-in-dB response. The curves above were obtained from an LMV225 and show that over the temperature range, the output voltage changes linearly for an input power level change from -55 dBm. To depict how linear the detection curve is, an error curve with respect to a fitted linear curve also is plotted for the same temperature range.

Typical Application LMV225, LMV226, and LMV228



The LMV225 detector is especially suited for power measurement via a high-resistive tap. The constant input impedance of the LMV225 (50Ω) enables the realization of a frequency-independent input attenuation to adjust the LMV225's range (-30 dBm to 0 dBm) to the power range of the PA. The attenuation realized is $20 \times \log(1 + R1/50\Omega)$. Parasitic capacitance of resistor R1 can impact the actual realized attenuation.

The LMV226/28 also have a 50Ω input resistance, but are designed to work with directional couplers that have attenuation. Therefore, the input range for these devices is -15 dBm to +15 dBm. The typical attenuation of a directional coupler is 20 dB, and so the LMV226/28 can be directly connected via the directional coupler to the PA without the need of additional external attenuation.

LMV225, LMV226, and LMV228 Specifications

- Logarithmic detector
- Log conformance error ± 2 dB
- RF frequency range 450 MHz to 2 GHz
- Supply voltage 2.7V to 5.5V
- Temperature range -40°C to $+85^{\circ}\text{C}$

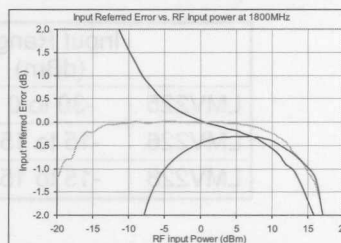
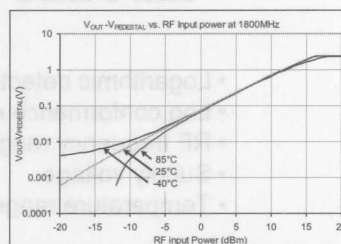
	Input Range (dBm)	Output Buffer	Application
LMV225	-30 to 0	No	High Resistive Tap
LMV226	-15 to 15	Yes	Directional Coupler
LMV228	-15 to 15	No	Directional Coupler



Mean-Square Detector

- Power applied to the input translates to a DC voltage on the output through a Logarithmic-in-dB response

- Power: X-axis = Logarithmic
- V_{OUT} : Y-axis = Logarithmic

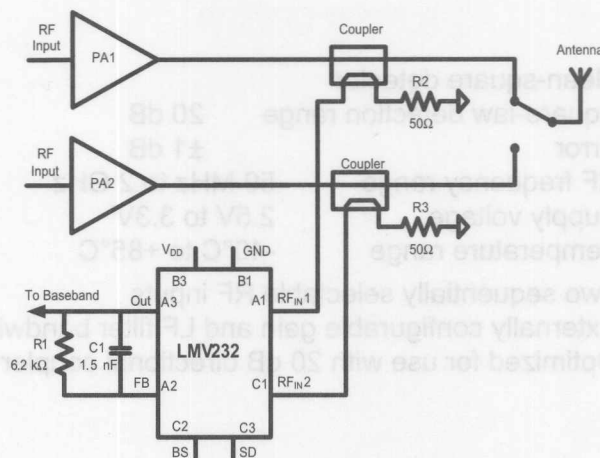


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The LMV232 is a mean-square detector and therefore has an output voltage (Volts) that relates logarithmically to the RF input power (dBm). The input referred error, with respect to an ideal linear mean square detector, is determined as a measure for the accuracy of the detector.

LMV232 Typical Application



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The LMV232 is especially suited for CDMA and WCDMA applications with two PAs. The output power of either PA can be measured at any time, depending on the position of the Band-Select (BS) pin. The measured output voltage of the LMV232 is read by the ADC of the baseband chip, and the gain of the PA is adjusted if necessary.

The LMV232 conversion gain is configured by resistor R1. A higher resistor value will result in a higher conversion gain. The maximum dynamic range is achieved when the resistor value is as high as possible: i.e. the output signal is just below clipping, while the voltage stays within the baseband ADC input range.

The two inputs of the LMV232 also can be used in an application with one PA to measure the transmitted power and reflected antenna power.

LMV232 Specifications

- Mean-square detector
- Square-law detection range 20 dB
- Error ± 1 dB
- RF frequency range 50 MHz to 2 GHz
- Supply voltage 2.5V to 3.3V
- Temperature range -40°C to $+85^{\circ}\text{C}$
- Two sequentially selectable RF inputs
- Externally configurable gain and LF filter bandwidth
- Optimized for use with 20 dB directional coupler

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Amplifier-to-ADC Interface

The amplifier must be able to drive the Analog-to-Digital Converter's (ADC's) input with minimum error. One challenge for the amplifier is that many ADC's have a switched capacitor on the input for sampling the amplifier's output. The amplifier must be designed for settling precisely with this type of load, or it will be necessary to find some way to isolate the ADC's input from the amplifier's output (see Section 2 on amplifier compensation).

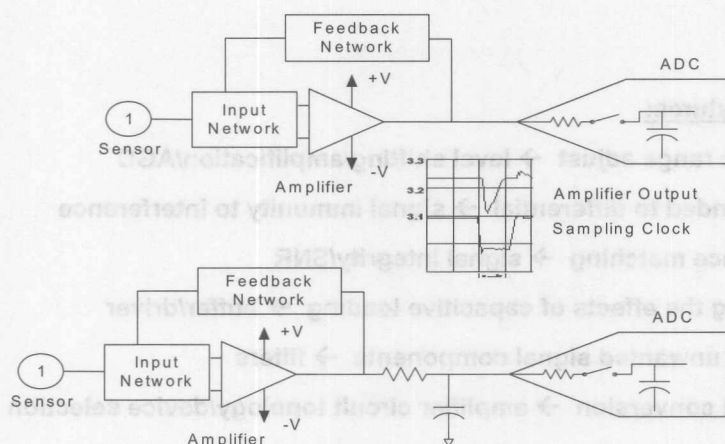
Driving the ADC

- **What load does the ADC present to the amplifier?**
 - **Most ADCs have a switched capacitor input**
 - **Amplifier's settling time**
 - **Amplifier's output impedance**
 - **Isolating the amplifier's output from the ADC input**



The amplifier must be able to drive the Analog-to-Digital Converter's (ADC's) input with minimum error. One challenge for the amplifier is that many ADCs have a switched capacitor on the input for sampling the amplifier's output. The amplifier must be designed for settling quickly with this type of load, or it will be necessary to find some way to isolate the ADC's input from the amplifier's output (see Section 2 on amplifier stabilization).

Amplifier-to-ADC Interface



Isolating the Amplifier from the ADC:
R and C values Dependent on Amplifier, ADC and Signal Frequency

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The top schematic shows the ADC's input connected directly to the output of the amplifier. When the sampling capacitor in the ADC is connected to the amplifier's output, a charging current flows from the amplifier to the ADC, which causes a momentary glitch that can take some time to settle. One way to minimize this effect is to slow down the sampling rate. This provides the amplifier with the time necessary to stabilize its output.

A second way to minimize the error caused by the switch capacitor is to have another capacitor connected to the ADC's input. This capacitor is much larger than the internal sampling capacitor and provides the charge needed to quickly charge the ADC's sampling capacitor. An isolation resistor is needed to isolate the additional load capacitance from the amplifier's output. In addition, the resistor and capacitor will form a low-pass filter and can be designed to provide noise reduction functions, as well as helping with the anti-alias function.

High-Speed Signal Paths

Basic Features:

- Dynamic range adjust → level shifting/amplification/AGC
- Single-ended to differential → signal immunity to interference
- Impedance matching → signal integrity/SNR
- Reducing the effects of capacitive loading → buffer/driver
- Remove unwanted signal components → filters
- I-V or V-I conversion → amplifier circuit topology/device selection



Previous signal sources have emphasized the need for precision op amps to provide the interface to the ADC. When the interface to the converter is required to handle high-speed signal sources, there are other things to be considered.

As before, the op amp is required to match the dynamic range of the source to the input dynamic range of the converter. ADCs are normally fixed-gain devices, providing the best performance when the input signal level is just below, but not above full scale. For many Radio Frequency (RF) sources Automatic Gain Control (AGC) is needed, and for this purpose, National has Voltage Controlled Variable Gain Amplifiers (VCVGAs) such as the LMH6502/03/04 series described next. Some sources, ultrasound transducers for example, require this gain to be time-variable to compensate for the signal loss incurred by deeper penetrating scans.

Earlier we saw that many sources provide a differential output signal, with op amps performing the conversion from differential input to single-ended output. Now that many new ADCs have differential inputs, op amps are used to convert single-ended inputs to differential outputs. This conversion can be done with conventional op amps, but is more readily accomplished by use of a fully differential op amp, such as the LMH6550.

What is a VCVGA?

- Output varies with V_G (gain control input)
- Used to adjust amplitude of a signal
- Differential (LMH6502/03) or single-ended input (LMH6504)
- Linear in dB or linear in V/V

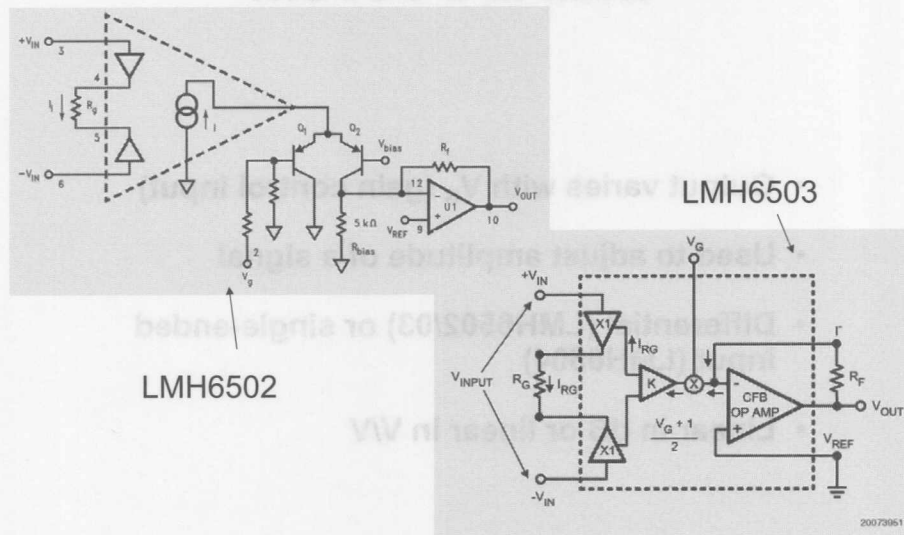


Before looking at differential drive to the ADC, we will consider the circumstances where the amplifier gain has to change dynamically in order to get the best performance out of the ADC. For broadcast radio applications, the distance between the transmitter and the receiver can vary greatly, and this means there are dramatic differences in the signal source amplitude. In ultrasound applications, there are large differences in the level of the reflected signal depending on the depth of penetration required. In these cases, it is common to use a Variable Gain Amplifier (VGA) to optimize the dynamic range at the input to the converter.

For a VGA, the output amplitude is a function of the input signal multiplied by the control voltage V_G . A linear change in this control voltage produces a linear change in gain, either in dB or in V/V. Sometimes, the gain control function is used to correct for a known gross amplitude degradation in order to allow for detection of a small signal (i.e. ultrasound).

As noted in the earlier section on RF detectors, sometimes it is preferable to have an output that is linear in dB with respect to the input.

LMH6502/03 Block Diagrams



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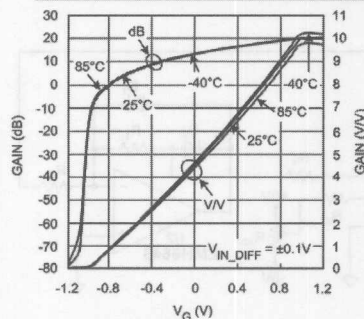
As you can see in the LMH6502 block diagram, the differential input to these devices is first buffered before being applied across an external resistor R_G . The current which flows in R_G , in response to the input differential voltage, is then sensed and applied to the tail current of the Q1, Q2 combination. By varying the base voltage of Q1 (V_G), one can control how much of the tail current flows through the 5 kΩ resistor on Q2 collector. This way, the signal gain can be varied. Q2 collector voltage is amplified using the CFA (U1) to appear at the output.

National's VGA's use a Gilbert cell to vary the GM of a differential amplifier with V_G . This will allow the signal to be fully attenuated (gain of 0), or fully on (maximum gain). The Gilbert cell output is then amplified by a Current-Feedback Amplifier (CFA). This achieves a bandwidth that is nearly independent of the gain setting or the amplitude of the output voltage.

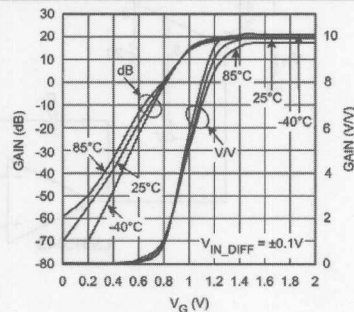
The LMH6503 functions in much the same way with the difference that there is additional circuitry that converts the logarithmic relationship of the LMH6502 to a linear one.

What is Linear in dB and Linear in V/V?

- Both have full range of gain (max gain to cutoff)
- Linear in dB (LMH6502 and LMH6504) allows more resolution at lower gains (e.g. AGC)
- Linear in V/V (LMH6503) is for applications where linearity in gain is more important (e.g. ultrasound)



LMH6503



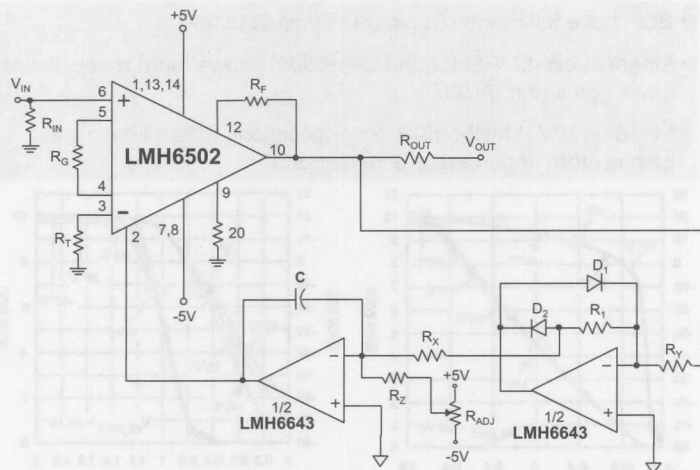
LMH6502



The main difference between the LMH6503 and LMH6502/04 is the gain control relationship. The LMH6503's gain control is linear in V/V and the LMH6502's gain control is linear in dB. These plots, taken from the LMH6503/04 datasheets will help explain the differences.

The first plot is taken from the LMH6503 datasheet and illustrates gain (V/V) vs. V_G . As you can see, the curve is linear over most of the V_G range. This is why we refer to the LMH6503 gain control as linear in V/V. The second gain curve plots the gain in dB and is linear over a wide range of gains. Because of this, the LMH6504 gain control is referred to as "linear in dB."

LMH6503 Typical AGC Circuit



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An Automatic Gain Control (AGC) circuit is a typical application for VGAs. A typical AGC circuit consists of a VGA and a feedback loop that performs integration and rectification to provide a control voltage V_G .

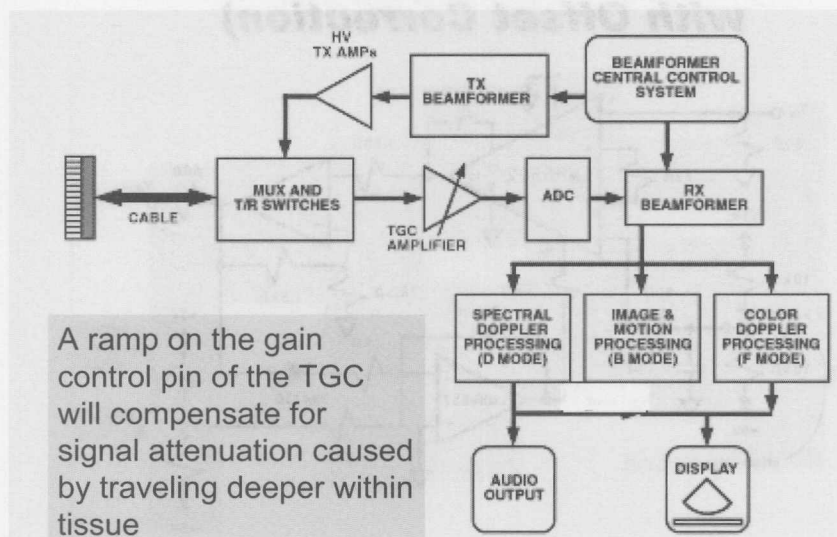
Circuit Description:

The dual amplifier LMH6643 is used to drive the gain control pin of the LMH6502. R_1 and R_Y set the gain of the rectifier. R_X , R_Y , and C provide a time constant that sets the acquire and hold times. The adjustable resistor, R_{ADJ} , sets the inverting pin of the integrator to the initial condition of +1V. When the RMS current of the signal is greater than the negative current of R_{ADJ} , the integrator decreases the gain of the LMH6503. And when the signal drops below the R_{ADJ} current, the LMH6503's gain is increased.

[illegible]

The gain of the LMH6714 stage eases the requirement on the LMH6502 max gain.

Ultrasound Block Diagram



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Here the VGA is used in the Time Gain Control (TGC) block shown above. The function of this block is to compensate for the loss of received signal as a function of the total round-trip time. The longer this time, the smaller the amplitude and the larger gain is required from the VGA.

There is a direct correlation between the receive delay and the distance to the object. The reason for this is that longer delays are associated with signals being returned from deeper tissue within the body. These farthest reflections are attenuated the most and require the highest gain.

This type of TGC amplifier needs linear-in-dB gain control (LMH6502 or LMH6504) and requires at least a 50 dB adjustment range. In addition, the VGA should have low noise and low distortion. Both devices mentioned are capable of meeting the requirements.

LMH6502/03/04

Variable Gain Amplifiers

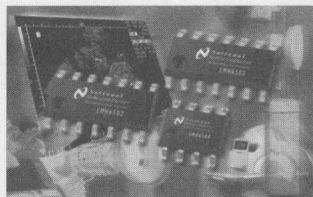
LMH6502/03 Variable Gain Amplifier

- 130 MHz signal bandwidth
- 100 MHz Gain control bandwidth
- >70 dB Gain adjustment range
- 1,800 V/ μ s slew rate
- Device-to-device gain matching within ± 0.7 dB
- ± 75 mA Linear output current
- 5V to 12V Supply voltage
- Replacements for CLC520/522
- Available in TSSOP-14 and SOIC-14 packaging

Ideal for automatic gain control applications in test, measurement, and instrumentation equipment, video communications, and medical imaging

LMH6504 Variable Gain Amplifier

- 150 MHz Signal bandwidth
- 150 MHz Gain control bandwidth
- 1,500 V/ μ s Slew rate
- Device-to-device gain matching within ± 0.42 dB
- 11 mA Supply current
- Gain control is linear in dB
- Replacement for CLC5523
- Available in MSOP-8 and SOIC-8 packaging



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This slide summarizes the main characteristics of the LMH65xx series of VCVGAs. They have been designed as improved replacements for the CLC520/22 with which some of you may have been familiar.

Differential Input Amplifiers

This slide summarizes the main characteristics of the LM102 and LM103. They have been designed as matched replacements for the LM102 and LM103 with which you may have been familiar.

Differential Amplifier with Common-Mode Feedback

- Uses three inter-related amplifiers
- Transfer function is:
 - $V_{OUT+} = (V_{IN+} - V_{IN-}) \times A_{IN} + V_{CM}$
 - $V_{OUT-} = -(V_{IN+} - V_{IN-}) \times A_V + V_{CM}$
 - $V_{CM} = V_{OCM} \text{ (input pin)} \equiv (V_{OUT+} + V_{OUT-})/2$
- Fully supports single-to-differential conversion because common-mode amplifier “drives” unused input
- Examples LMH6550, LMH6551

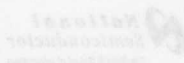


The “driven” input is one key benefit of the common-mode amplifier since without the common-mode amplifier the ADC input suffers a 6 db gain loss. Maybe even more importantly, it loses 6 dB of dynamic range.

For driving an ADC, the other benefit of the common-mode amplifier is that it allows the output common-mode of the amplifier to be precisely set to the best value for the driven ADC.

Differential Amplifier with Common-Mode Amplifier

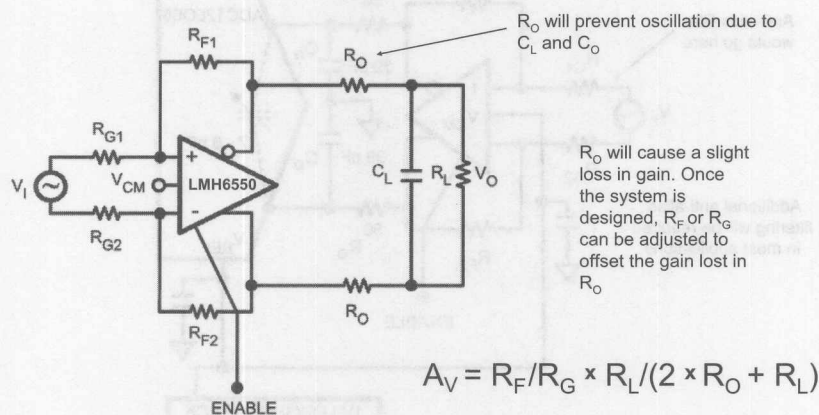
- Output common mode is now variable and user defined. Can be fixed or an AC signal
- Most flexible differential amplifier in existence
- Exceptionally well-suited to driving ADCs
- Inputs are virtual short, but NOT virtual ground
- Common mode of input is set by output common mode and feedback divider effect – can cause problems with single supply and high gain
- Common mode at output will set up DC currents, especially in single-supply operation



The "driven" input is one key benefit of the common-mode amplifier since without the common-mode amplifier the ADC input suffers a 6 dB gain loss. Maybe even more importantly, it loses 6 dB of dynamic range.

For driving an ADC, the other benefit of the common-mode amplifier is that it allows the output common-mode of the amplifier to be precisely set to the best value for the driven ADC.

Basic Application



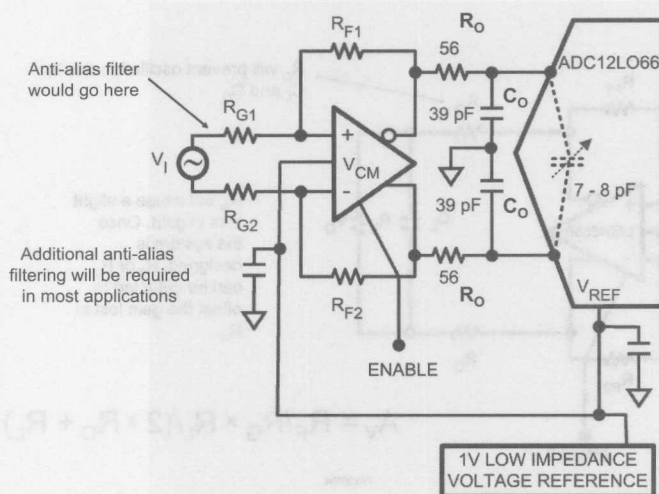
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A split supply provides best performance and maximum flexibility. In the above schematic, power supply and bypassing capacitors are not shown for clarity. Standard ceramic chip capacitor bypassing is mandatory for all high-speed amplifiers with 0.01 μF as a good value for the bypass capacitors.

For the typical ADC, C_L is around 7 to 12 pF and R_L will be from 1 k Ω to near infinity. R_O is necessary for most of the ADCs that are suitable for use with this part (LMH6550). Most designs will include an external capacitor C_O to help provide current to charge the sampling capacitance C_L .

Driving an ADC



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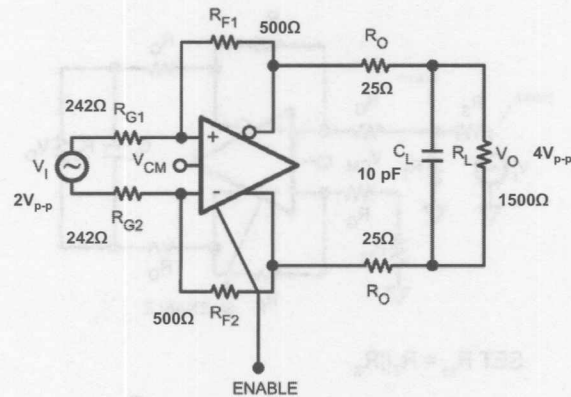
R_O (56Ω resistor) is needed to prevent the amplifier from oscillating with the ADC load. C_O (39 pF) is recommended to help shunt the currents associated with the sample-to-hold transition from the ADC front end. Since R_O and C_O are needed anyway, they can be used to help implement the anti-alias filter (not shown). They will form a low-pass filter with a cut-off frequency given by

$$F_{\text{cutoff}} = 1 / (2 \times \pi \times 56\Omega \times (39 \text{ pF} + 14 \text{ pF}))$$

** Note using 14 pF = double the actual ADC input capacitance – this is due to the differential circuit.

The V_{REF} output of some CMOS amplifiers cannot drive the V_{CM} input of the LMH6550. An external reference or a buffer amplifier is required in that case.

Adjusting R_G to Compensate for R_O



$V_S = \pm 5V$, $V_{CM} = 0V$
 $R_F = 500\Omega$, $R_G = 250\Omega$, $R_O = 25\Omega$, $R_L = 1500\Omega$,
 $C_L = 10\text{ pF}$
 $A_V = 500/242 \times 1500/1550 = 1.999\text{ V/V}$

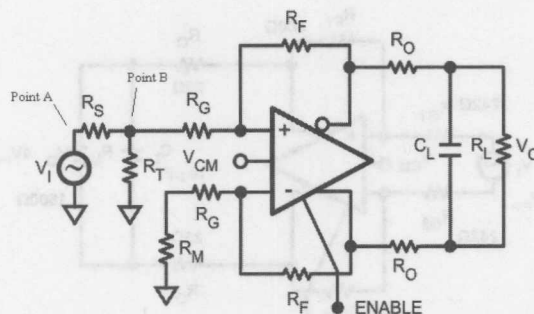
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The differential amplifier datasheet will specify the minimum value of R_O needed to stabilize the amplifier output for a given capacitive load. This value can be adjusted slightly if desired to help form an output filter.

Check the ADC datasheet for the input resistance. Some ADCs will be very high resistance and will require little or no adjustment of R_G .

Single-Ended Operation



$$\text{SET } R_M = R_T || R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} + \frac{1}{R_{IN}}\right)}$$

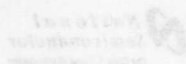
$$R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 * (R_F + R_G)}\right)}$$

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These equations need to be solved iteratively. You first calculate R_{IN} ignoring the effects of R_T and R_M . If R_M is large enough, it will change R_{IN} and the equation will need to be solved again. Given 1% resistors, two iterations should suffice.

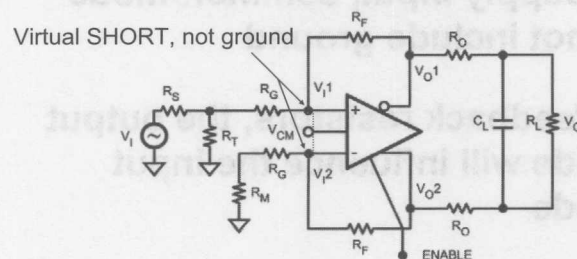
Common-Mode Importance

- **With single-supply input, common-mode range does not include ground**
- **Because of feedback resistors, the output common mode will influence the input common mode**
- **Signal-source common mode also will influence amplifier input common mode**



This is one of the biggest design challenges for the differential amplifiers. Using a single-ended input on single supply requires close attention to the amplifier input-range specifications. The next few slides will detail two example calculations.

Common-Mode Calculation



$$*V_{CM} = \frac{V_{O1} + V_{O2}}{2} \quad *BY\ DESIGN$$

$$V_{ICM} = V_{OCM} \cdot \frac{(R_G + R_M)}{(R_G + R_M + R_F)} \approx \frac{V_{OCM}}{1 + A_v} \quad \text{WHERE } R_M \ll R_G$$

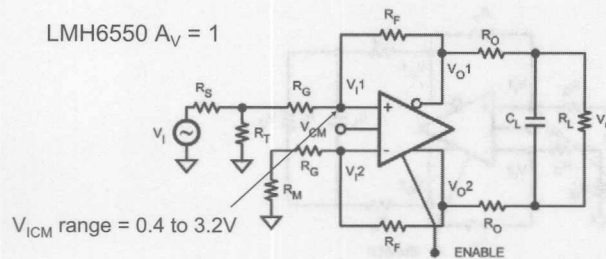
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If V_I has a common-mode voltage, then by superposition, it will add to the V_{CM} voltage. These calculations are for $V_{ICM} = (V_{I1} + V_{I2})/2$. This is necessary to make sure that the input common-mode range of the amplifier is not violated.

Single-Supply Common Mode Example 1

LMH6550 $A_V = 1$



Given, $V_S = +5V$, $V_{CM} = 2V$, $R_F = 500\Omega$, $R_G = 500\Omega$, $R_S = 200\Omega$

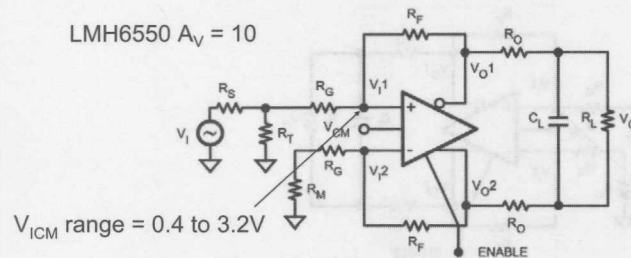
Then, $R_{IN} = 667\Omega$ so set R_T to 285Ω and R_M to 118Ω V_{ICM} then = $1.1V$



If V_{ICM} is $1.1V$, the input pin is well away from the limit of $0.4V$. This assures good linear operation and the ability to handle large input signals.

Single-Supply Common Mode Example 2

LMH6550 $A_V = 10$



Given, $V_S = +5V$, $V_{CM} = 2V$, $R_F = 1090\Omega$, $R_G = 109\Omega$, $R_S = 200\Omega$

Then, $R_{IN} = 200\Omega$ so R_T is not needed and $R_M = 0\Omega$

V_{ICM} then = 0.2V – Amplifier is not operational at this V_{ICM}



In this case, the amplifier is not operational. Additionally, the amplifier will not achieve datasheet distortion and swing performance if V_{ICM} is too close to 0.4V. If the input signal goes below ground, then the input common mode will be pulled even lower.

Common Mode Example 3

Solutions for Input Common Mode Problems:

- **Use split supplies**
- **Use two amplifiers with gains of 3.16**
- **Raise output common mode and AC couple**



High gain can be supported without any problem on split power supplies. As gain goes up, the input common mode is driven toward zero volts. On split supplies, a zero volt input common mode is a valid operating state.

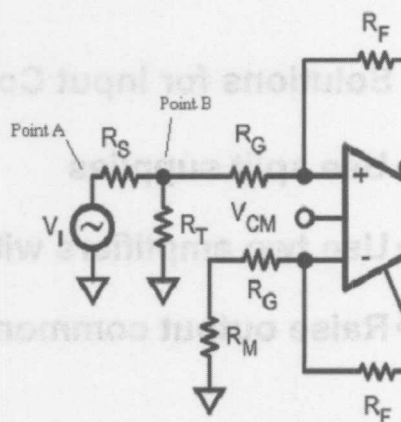
Solution number 2 is based on the fact that as gain goes down, the input common mode is closer in value to the output common mode. In this case, it is suggested to use the square root of 10 to split the gain equally between the two amplifiers. This is not strictly necessary, but is a good first suggestion.

Of course, AC coupling is probably not an option in most cases where a differential amplifier is used. There are still advantages over a transformer, though. Transformers usually have trouble coupling below 100 kHz, whereas with AC coupling, it is possible to use large capacitors and get performance down to tens of kilohertz.

Single-Ended Operation

GAIN – Two Definitions

1. $\frac{1}{2} \times R_F/R_G = \text{Gain from Point A (system level)}$
2. $R_F/R_G = \text{Gain from Point B (Amplifier Definition)}$



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The datasheet specifications were determined with point B as the reference point. This is because most high-speed signal sources are 50Ω devices making point A internal to the test equipment and unavailable for probing. Internal source resistance is also usually calibrated out and again not available for inspection. Point B marked the evaluation board connector.

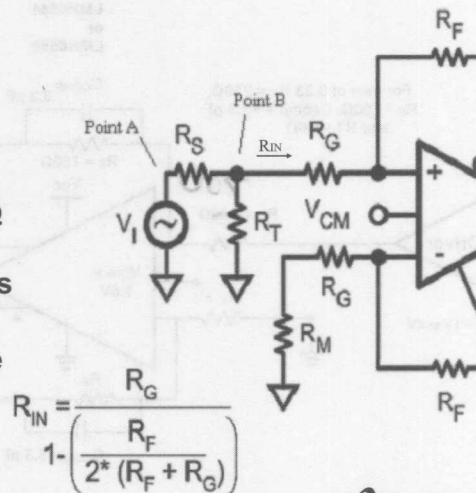
Systems designers, on the other hand, are usually interested in overall system performance. So it is important to realize that with impedance matching, there is a voltage loss between the two stages. One way around this is to have the source placed very close to the amplifier and to not use impedance matching. In this case R_T and R_M can be eliminated and the upper R_G can be reduced so that R_S becomes part of R_G .

Single-Ended Operation

Performance Hints

- Smaller R_F and R_G will reduce bandwidth and peaking
- For higher gains use larger R_F , try to keep R_G between 100Ω and 300Ω
- R_T and R_M can be eliminated if R_{IN} matches R_S ($R_G > R_S$)
- Not All R_S values can be matched

R_{IN} equation does not include effects of R_T and R_S .

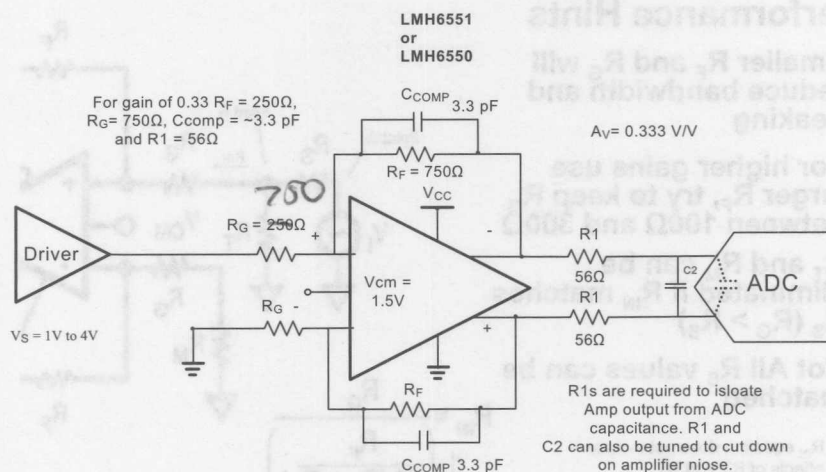


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The ideal value of R_G is around 300 to 500 Ω . At lower gains R_F should be kept around 500 Ω . For higher gains R_F should be increased, rather than decreasing R_G . At higher gains, peaking will not be as much of a problem.

Input impedance values greater than R_{IN} cannot be matched. This is because the differential configuration has no high impedance inputs.

Single Supply with Frequency Compensation



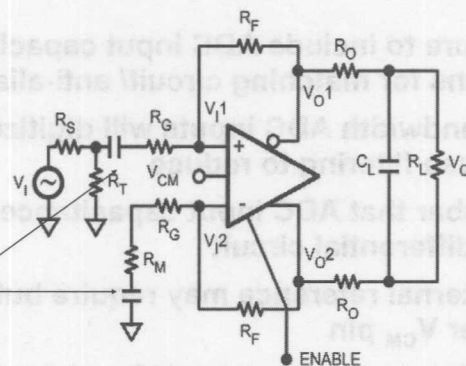
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With differential amplifiers, gains of less than 1 are possible, but may cause unacceptable peaking of the frequency response. Choosing a value of C_{COMP} that has a reactance of around 2x the resistance of R_G at the frequency where peaking is observed is a good starting point. In this example C_{COMP} has reactance roughly equal to the resistance of R_G at the frequency where peaking was observed. In this example, the customer was interested in a flat response more than bandwidth.

Single-Supply Operation AC Coupled

AC coupling allows higher gain and lower output common mode voltages

* $V_{ICM} = V_{OCM}$
because of
capacitive
isolation.



$$*V_{CM} = \frac{V_{O1} + V_{O2}}{2}$$

*BY DESIGN

$$V_{ICM} = V_{OCM}$$

$$V_{ICM} = \frac{V_{I1} + V_{I2}}{2}$$

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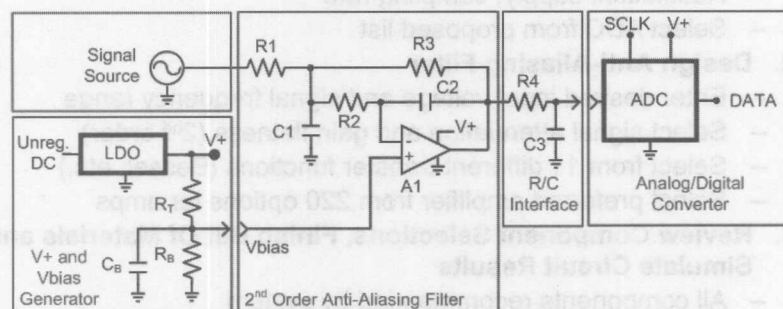
NOTE!! The equation $V_{ICM} = V_{OCM}$ is valid only because of the capacitors between R_T , R_G , R_M , and ground.

Driving an ADC

- Make sure to include ADC input capacitance in equations for matching circuit/ anti-alias filter
- High-bandwidth ADC inputs will digitize amplifier noise: use filtering to reduce
- Remember that ADC input capacitance will be doubled due to differential circuit
- ADC internal reference may require buffer to drive amplifier V_{CM} pin
- ADC reference voltage (and V_{CM} pin voltage) is critical to ADC operation. Check amplifier common mode calculations to see if split-supply operation of amplifier is required



Designing Anti-Aliasing Filters with WEBENCH® Online Tools



For many amplifier/ADC interfaces, the op amp is used to implement the anti-alias filter. To help the design procedure, National has expanded its WEBENCH® online tool offerings. The Signal Path Designer tool combines ADC selection with the design of an anti-aliasing filter. In addition, a simple resistor-capacitor interface circuit is customized for the application.

WEBENCH® Signal Path Designer Tool Selection Process

1. Set ADC Performance Requirements

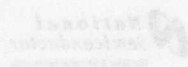
- Resolution, supply, sampling rate
- Select ADC from proposed list

2. Design Anti-Aliasing Filter

- Enter desired input voltage and signal frequency range
- Select signal attenuation and gain flatness (2nd order)
- Select from 11 different transfer functions (Bessel, etc.)
- Select preferred amplifier from 220 options for amps

3. Review Component Selections, Finish Bill Of Materials and Simulate Circuit Results

- All components recommended by system
- Review calculated system performance

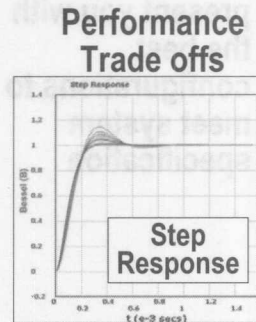
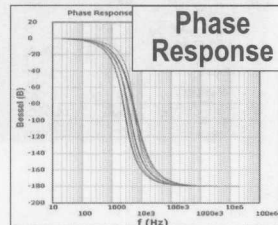
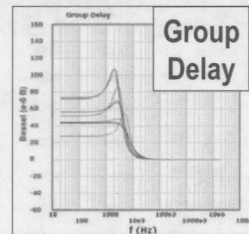
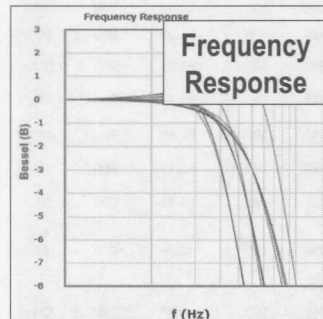


In the WEBENCH® Signal Path Designer tool, requirements for the data sampling are identified, which leads to selection of an ADC from a list of candidates. The 2nd order anti-aliasing filter is designed next, based on the input signal characteristics and desired filter response. As in the Active Filter Designer tool, the ideal filters are evaluated first, then one is selected for implementation. An amplifier is selected for use in the active filter based on the system requirements.

The overall circuit, including the selected components, is presented to the user. The user can review the circuit performance and make adjustments to the ADC's input voltage range and resistor tolerances. When the operating value calculations look good, the user can electrically simulate the filter.

Choose Ideal Performance Envelope For Your Needs

Review filter response across
frequency, phase, group delay,
and step response



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In addition to frequency response, it is often helpful to evaluate the filters by their group delay or step response. Sometimes a filter with a very sharp, near-ideal frequency response will have a step response with a lot of ringing. This will indicate a filter that may not settle quickly from an input transient, making it difficult to accurately sample a suddenly-changing input signal.

Select The Ideal Filter For Your Needs

20,000 iterations
per filter response
present you with
the best
configurations to
meet system
specification

Response	Filter Reference Frequency (Hz)	Max Signal Frequency (Hz)	Gain Flatness Error up to Fmax (dB)	Nyquist Frequency (kHz)	Attenuation at Nyquist (dB)	Selected Sample Rate (ksps)	Min Nyquist Sample Rate (ksps)
<input type="radio"/> Bessel	5000	2000	0.4426	100	47.98	200	126
<input type="radio"/> Butterworth	4000	2000	0.2586	100	56.04	200	80
<input type="radio"/> Chebyshev 1dB	7000	2000	0.3944	100	48.88	200	122
<input type="radio"/> Chebyshev 0.5dB	4000	2000	0.4992	100	58.14	200	72
<input type="radio"/> Chebyshev 0.25dB	3000	2000	0.2501	100	62.68	200	56
<input type="radio"/> Chebyshev 0.1dB	3000	2000	0.4157	100	62.17	200	56
<input checked="" type="radio"/> Chebyshev 0.01dB	4000	2000	0.1801	100	56.44	200	78
<input type="radio"/> Equiripple 0.5° error, Linear Phase	5000	2000	0.2925	100	50.4	200	110
<input type="radio"/> Equiripple 0.05° error, Linear Phase	5000	2000	0.3992	100	48.87	200	120

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For the more analytical designers, a chart is provided that summarizes the numerical aspects of the ideal filter's performance. In this table, it can be seen that to achieve the same gain flatness and the same attenuation at Nyquist, the different response approximations need to have different reference frequencies.

In addition, to support the specified maximum signal frequency, some of the responses have more attenuation at FN than is necessary. Their sample rates could be reduced and the other performance requirements would still be met.

Select one filter response from this table to be implemented.

Review Suggested Amplifiers For Your Anti-Aliasing Filter

Recommended Parts

Product Folder Datasheet 24 Hour Samples Samples Buy Now

NOTE: An attribute highlighted in RED indicates that this product is not a direct match.

Part Number	Pkg	Bandwidth at Closed Loop Gain of 2 (MHz)	Feedback Type (voltage or current)	Min. Closed Loop Gain (V/V)	Max. Supply Voltage (V)	Min. Supply Voltage (V)	Input Offset Voltage, typ at 25C (mV)	Gain-Bandwidth Product, typ (MHz)	Supply Current typ per channel (mA)	Number of Channels	Min. Open Loop Gain (V/mV)	Min. Operat Temp (degC)
<input type="radio"/> LPV321M5 LPV321.MOD		0.076	VFB	1	5	2.7	1.5	0.152	0.009	1	100	-40
<input type="radio"/> LPV321M7 LPV321.MOD		0.076	VFB	1	5	2.7	1.5	0.152	0.009	1	100	-40
<input type="radio"/> LMP2011MF LMP2011.MOD		1.5	VFB	1	5	2.7	0.0008	3	0.93	1	3160	0
<input type="radio"/> LMP2011MA LMP2011.MOD		1.5	VFB	1	5	2.7	0.0008	3	0.93	1	3160	0
<input type="radio"/> LMV2011MA LMV2011.MOD		1.5	VFB	1	5	2.7	0.0008	3	0.93	1	3160	0
<input type="radio"/> LMV2011MF LMV2011.MOD		1.5	VFB	1	5	2.7	0.0008	3	0.93	1	3160	0
<input type="radio"/> LMV341MG LMV342.MOD		0.5	VFB	1	5	2.7	0.025	1	0.107	1	630	-40
<input checked="" type="radio"/> LMV342MM LMV342.MOD		0.5	VFB	1	5	2.7	0.7	1	0.107	2	630	-40

Select op amp

Excellent
performance
National Semiconductor

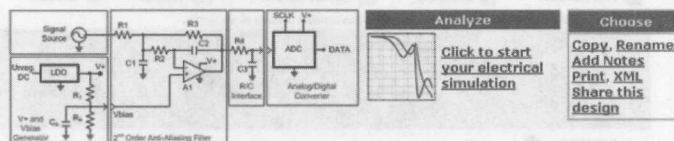
National Semiconductor
The Sight & Sound of Information

The next step in implementation is to choose the op amp to be used in the anti-aliasing active filter. The op amps in this list are selected to meet the bandwidth, closed-loop gain, and supply-voltage requirements of the design. Also in general, those with lower input offset voltage, lower supply current, and gain-bandwidth close to the desired target will be higher on the list.

Although the list initially contains 10 amplifiers, many more may be candidates. If this is the case, there will be a link at the bottom of the table to display all the candidate amplifiers.

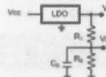
Finalize Design Review and Component Selections

ADC Channel Design Summary



Bias Divider Section

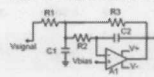
Bias Divider



Components		
Cb	5e-07 uF	
Rb	14.3 kOhm	1 %
Rt	35.7 kOhm	1 %

Section A

AAF MultipleFeedback AAF FirstOrder_RC



Components		
A1	LMV342MM	
C1	0.068 uF	
C2	0.0082 uF	
R1	1.18 kOhm	
R2	866 Ohm	
R3	3.16 kOhm	

Section B

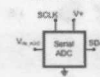
RC FirstOrder_RC



Components		
C3	0.0004 uF	
R4	22 Ohm	

ADC Section

Serial ADC



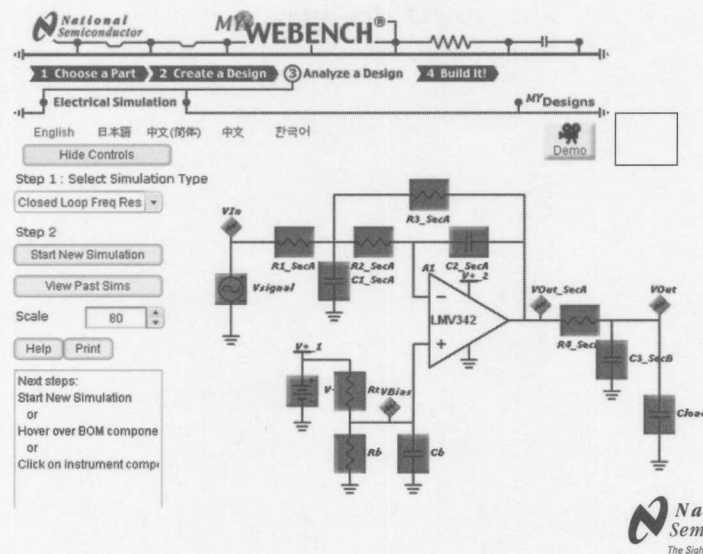
Components		
ADC1	ADC102S021CIMM	



Now that the ADC is selected and the anti-aliasing filter is designed, the remaining circuit elements are calculated. Because the anti-aliasing filter is operating from a single (ground-referred) supply voltage, a bias voltage is needed to bring its output voltage into the ADC's operating input voltage range. This bias voltage is constructed using the system supply voltage, divided down with two resistors, Rb and Rt, and filtered with a capacitor Cb.

Also, the ADC input is capacitive, and the capacitance varies as it switches into and out of sample mode. This would present a changing load to the filter amplifier, potentially reducing its stability. The simplest interface between amplifier and ADC is a series resistor, parallel capacitor. These components are automatically calculated to minimize the effect of the changing ADC input capacitance.

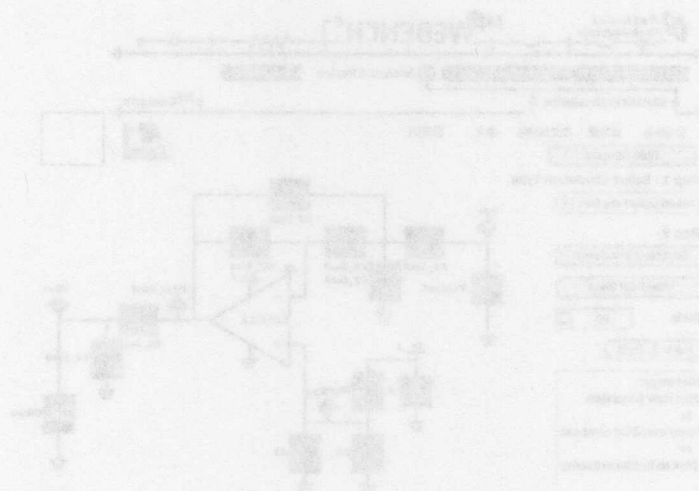
Circuit For Simulation and Evaluation



The electrical simulation is for the filter and R-C interface circuits. Available tests include frequency response and step response, as well as a sine-wave response, to verify operating voltages in the circuit.

If you are unfamiliar with this simulation environment, click the “Demo” button to see a brief tutorial video.

Circuit for Simulation and Evaluation



National
Instruments

The simulation is for the first two R-C network circuits. Available test results: frequency response and step response, as well as a time wave response, to verify operating behavior in the circuit.

If you are unfamiliar with the simulation environment, click the "Guide" button to see a brief tutorial video.

Data Conversion Systems

Analog-to-Digital Converters (ADCs) are conceptually simple: give them an analog voltage (or current) and they give you a digital word. Practical application of ADCs is, however, not quite so simple.

Most of us are more comfortable using a DAC than using an ADC, but even the DAC does have areas about which we should be careful.

Here we will discuss concrete ways to get the best performance from these products, including examples of customer problems and how they were resolved.

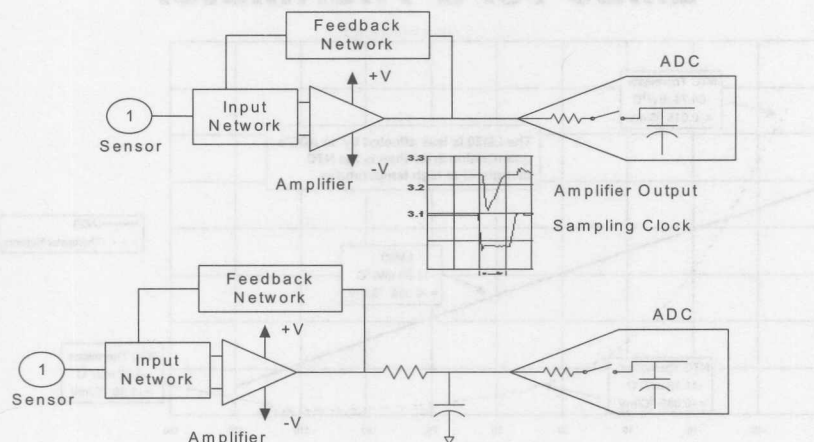
Semiconductor Temperature Sensors

Most of us are more comfortable using a DAC than using an ADC, but even the DAC does have areas where we should be careful.

Here we will discuss concrete ways to get the best performance from these products, including examples of customer projects and how they were resolved.

Analog-to-Digital Converters (ADCs) are conceptually simple: give them an analog voltage (or current) and they give you a digital word. Practical application of ADCs is, however, not quite so simple.

Amplifier-to-ADC Interface



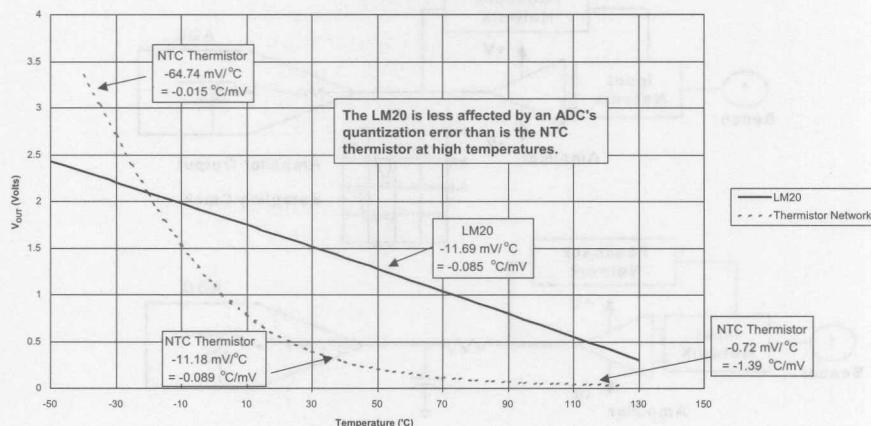
Isolating the Amplifier from the ADC:
R and C values Dependent on Amplifier, ADC and Signal Frequency

National Semiconductor
The Sight & Sound of Information

The top schematic shows the ADC's input connected directly to the output of the amplifier. When the sampling capacitor in the ADC is connected to the amplifier's output, a charging current flows from the amplifier to the ADC, which causes a momentary glitch that can take some time to settle. One way to minimize this effect is to slow down the sampling rate. This provides the amplifier with the time necessary to stabilize its output.

A second way to minimize the error caused by the switch capacitor is to have another capacitor connected to the ADC's input. This capacitor is much larger than the internal sampling capacitor and provides the charge needed to quickly charge the ADC's sampling capacitor. An isolation resistor is needed to isolate the additional load capacitance from the amplifier's output. In addition, the resistor and capacitor will form a low-pass filter and can be designed to provide noise reduction functions, as well as helping with the anti-alias function.

Transfer Function Comparison LM20 vs. a Thermistor



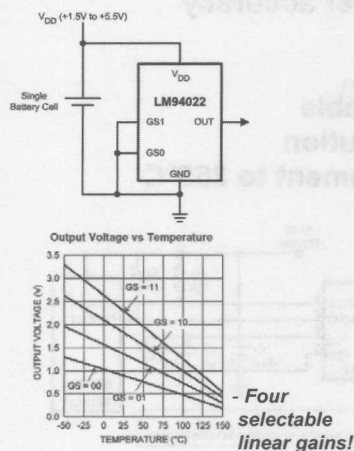
**National
Semiconductor**
The Sight & Sound of Information

When driving the input of an ADC from the output of a temperature sensor, it is important to realize that every ADC has a quantization error associated with it. The higher the resolution of the ADC (the more bits it has), the smaller the quantization error. When digitizing the output of an analog temperature sensor, this quantization error translates directly into a temperature-reading error – the higher the quantization error (the lower the ADC resolution), the higher the temperature-reading error.

The slope of the temperature sensor's transfer function (change in voltage per change in temperature) determines how severe of an impact the ADC error will have upon the temperature measurement. Let's say that an 8-bit ADC has a reference of 5V so that each LSB is equal to about 19.5 mV. The LM20, as an example, has a slope of -11.69 mV/°C. This is equivalent to -0.085 °C/mV, which means that one LSB of quantization error would result in a maximum $(0.085 \text{ °C/mV} \times 20 \text{ mV}) = 1.7^\circ\text{C}$ error.

Consider now that the NTC thermistor has a slope of -64.7 mV/°C at -35°C. Its temperature error due to quantization would be 0.30°C error at this cold temperature. However at 120°C, the thermistor has a slope of -1.39°C/mV. So it would have a digitized temperature error of 27.8°C! The plot above shows that National's LM20 performs better at temperatures above about 35°C, the point where the thermistor has approximately the same slope as that of the LM20. Also, National's LM94021 has four possible gains; so, the quantization error can be managed by simply changing the gain.

LM94022: Lowest Supply Voltage



- **1.5V to 5.5V Supply**
- Next generation following LM20
- 5.4 μ A typ Quiescent current
- $\pm 1.5^\circ\text{C}$ Accuracy
- -50°C to 150°C Operating temperature
- SC70 Package
- Four selectable gains to optimize maximum gain for a given supply voltage
- Optimized to drive ADC inputs
 - 50 μ A Output Source Current
 - 1100 pF Load Capacitance without external resistor
- Competitor's Supply Voltage
 - Seiko S8110: 2.4V min
 - Maxim MAX6613: 1.8V min



National's LM94022 is a next-generation LM20 temperature sensor. Besides an industry-leading minimum supply voltage of 1.5V, it has many excellent specifications and comes in a tiny SC-70 package, making it ideal for small, portable products such as cell phones.

The low 5.4 μ A (typical) supply current preserves battery power.

The LM94022's four selectable temperature-to-voltage gains allow the system designer to optimize the design to get the highest gain over the system's operating temperature and supply voltage. Selecting the lowest gain allows the LM94022 to measure temperature in a low-voltage system such as the 1.8V supplies for 90 nm processes used by many controllers and ASICs, providing a temperature-analog signal over the full operating range of -50°C to 150°C . For systems with higher supply voltages, all the advantages of a steeper output slope can be utilized by selecting a higher gain.

The LM94022 has been optimized to drive ADC inputs by providing the ability to output 50 μ A of current and the capability to drive 1100 pF of load capacitance without the need for external resistors or buffers.

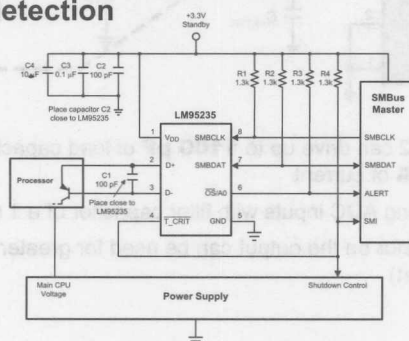
- **TruTherm technology for better accuracy**
- **SMBus interface**
- **Two remote diode capability**
- **Three address versions available**
- **Up to 13-bit (0.03125°C) resolution**
- **Remote temperature measurement to 255°C**
- **Diode fault detection**



The diode fault-detection circuit reports a fault condition if the D+ pin is shorted to GND, to D-, to the supply, or is floating.

LM95235 TruTherm™ Remote Diode Temperature Sensor

- TruTherm technology for better accuracy
- SMBus interface
- Three-level address pin
- Up to 13-bit (0.03125°C) resolution
- Remote temp measurement to 255°C
- Diode fault detection



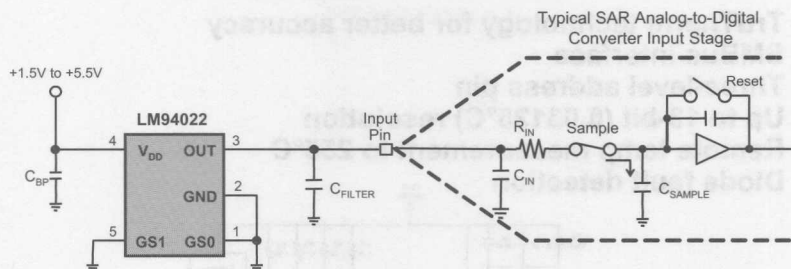
National Semiconductor
The Sight & Sound of Information

The LM95235 is very similar to the LM95241 except that, rather than using three different versions for different addresses, a three-level address pin is used to provide the possibility of three different LM95235s on the same bus. It also can measure the temperature of a single remote diode in addition to its own die temperature.

Pin 6 is programmed to be an address input or an active low "Over Temperature Shutdown" output that can be used to shut the system down, interrupt a processor, or any desired function when temperature exceeds a pre-programmed limit.

The LM95241 and the LM95235 are just two examples of the remote diode temperature sensors available from National.

Application Consideration: Driving ADC Inputs



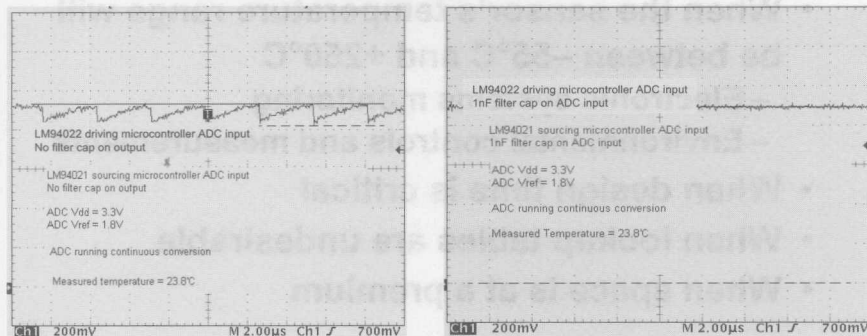
- The LM94022 can drive up to **1100 pF** of load capacitance and source **50 μ A** of current
- Ideal for driving ADC inputs with filter capacitor of a 1 nF or less
- A series resistor on the output can be used for greater load capacitance (see datasheet)



Most analog temperature sensor applications use an ADC to sample the analog temperature-proportional voltage output. These ADCs may be discrete or may be integrated into a processor or a microcontroller. The LM94022's output is optimized for driving the input stage of an ADC and a filter capacitor that is often located at the ADC input. Its high 1100 pF max load capacitance specification means that a filter capacitor as large as 1 nF \pm 10% can be driven by the LM94022 without requiring any external series resistor to stabilize the output. Eliminating the extra component saves the customer cost and board space.

Additionally, the robust 50 μ A of source current is designed to drive demanding ADC current requirements.

Customer Problem: Inaccurate Temperature Reading



The "Measured Temperature" is measured with a separate sensor.



A customer complained of inaccurate temperature readings with the LM94022 when driving the input to a sampling ADC. In a cost-cutting move, he eliminated the capacitor at the LM94022 output.

These two scope photos demonstrate (1) the transient loads placed on the source when the ADC's sampling capacitor is charging and (2) the stability achieved by placing a filter capacitor at the input to the ADC. The capacitor is needed when the sampling rate is too fast to allow the temperature sensor output (ADC input) to stabilize. When the sensor is a low power device, as with the LM94022, it may not produce enough output current to settle before the sample is taken, and the addition of a filter capacitor will improve accuracy. The size of the capacitor will depend upon the size of the internal ADC sampling capacitor (in this case, the ADC sampling capacitor was approximately 50 pF) and also upon the sampling frequency. Generally, the filter capacitor value should be about 10 to 20 times the ADC sample capacitor value. Care must be taken to ensure that the sample frequency is matched to the maximum source current of the sensor so that the filter capacitor remains charged to the appropriate level. As you can see in the first image, the output gets pulled low as the sample capacitor starts to charge. If the sample rate is faster than the time in which the capacitor can be recharged, that capacitor would still be charging and not settled when the next sample time ends. The second image shows the benefit of adding a 1 nF filter capacitor at the ADC's input. The result is a stable DC voltage which is proportional to temperature.

We generally recommend a series resistor in addition to the capacitor for dynamic applications, but the capacitor alone can be used if the ADC input is static or a slowly moving DC and the driving device can tolerate the capacitance.

Note also that the "Measured Temperature" indicated here is the temperature measured with a separate sensor.

When Should You Use IC Temperature Sensors?

- When the sensor's temperature range will be between -55°C and $+250^{\circ}\text{C}$
 - Electronic systems monitoring
 - Environmental controls and measurements
- When design time is critical
- When lookup tables are undesirable
- When space is at a premium



Designers have numerous options for temperature sensing techniques. Thermistors, RTDs, thermocouples, and active silicon sensors are among the most common. Each has its own set of advantages and disadvantages in any given application. IC sensors have major advantages when the temperatures to be measured fall within the normal operating temperature range of silicon ICs. Among these advantages are small size and fast design time (because external signal conditioning circuitry is either minimal or not required). In addition, sensor ICs can include extensive additional functions, such as built-in trip-point comparators or digital I/O. And, since they include on-chip linearity correction, there is no need for lookup tables to correct for linearity errors.

National's Focus Areas in Temperature Sensors

- **Multiple Remote Diode Temperature Sensors (RDTS)**
 - LM83, LM95241, LM95235, LM95221, LM95231
- **Tiny, accurate temperature sensors for portable systems**
 - LM20, LM94022
- **Accurate temperature sensors**
 - LM73, LM76, LM92, LM95071



National has a wide variety of integrated circuit temperature sensors for many different uses. Traditionally used in Heating, Ventilation and Air Conditioning (HVAC) control systems, temperature sensors also can be found in PCs, PC peripherals and in personal communication devices and other communications equipment, to name just a few places. IC temperature sensors can measure the temperature of a printed circuit board, ambient air, chassis case temperature, and the die temperature of a power-hungry ASIC, graphics engine or CPU.

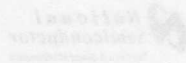
The latter is where RDTS has found the greatest use. Sensing the case temperature of power-hungry ICs has always had its mechanical challenges in terms of placement and mounting of the temperature sensor. If the IC is a surface-mounted device, it usually has hundreds of pins, making positioning of the external temperature sensor close enough to get an accurate, low thermal lag measurement a nightmare for PCB layout. National's RDTS products help solve these kinds of monitoring problems.

With the continued miniaturization of portable systems, National has led in the IC package miniaturization challenge. We have both analog and digital temperature sensors in micro SMD (Surface Mount Device) and LLP® (Leadless Leadframe Packages). Our 4-pin micro SMD package is smaller than many available surface mount resistors.

Applications in modern HVAC and process control systems require great accuracy. Again, National is the leader with the most accurate digital output temperature sensor available today.

Hardware Monitor Functions

- Temperature sensing
 - Local
 - Remote diode
- Other temperature sensors
- Supply voltages
- Any analog sensor



Hardware monitors are devices used to monitor the status of a system. As such, they contain an internal temperature sensor, remote diode temperature sensing capability, and inputs for other voltages that may come from supply voltages, analog temperature sensors, or any other type of sensor or voltage source.

The latest in what RDT has been the fastest and most accurate of power supply ICs has always had its mainstay in terms of placement and monitoring of the temperature sensor. If the IC is a surface-mount device, it usually has a number of pins, making positioning of the sensor more difficult. In fact, it's not an accident, but a design for measurement a highlight for RDT's latest RDT products help solve these kinds of mounting problems.

With the continued miniaturization of portable systems, National has led in the IC package miniaturization challenge. We have both analog and digital temperature sensors in tiny SMD (surface mount device) and 1.1mm (leadless package) packages. Our 4-pin SMD package is smaller than any available surface mount package.

Application is modern HVAC and process control systems require great accuracy. A great feature of the latest with the most accurate digital output temperature sensor available.

LM94 TruTherm™ Hardware Monitor

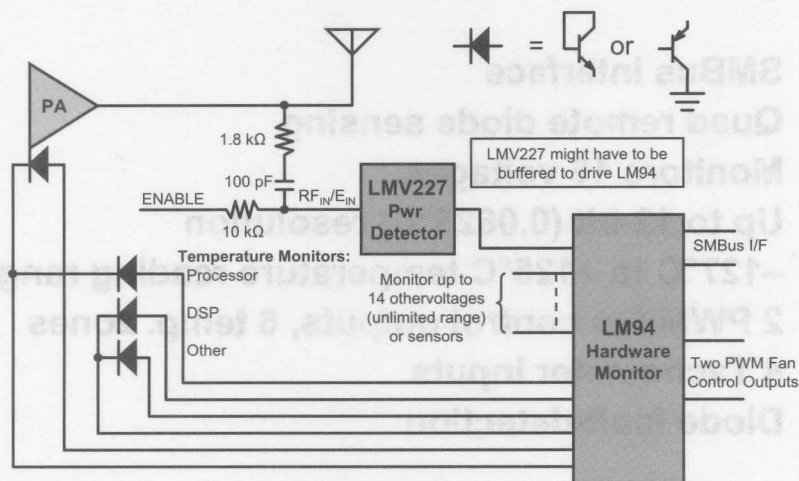
- SMBus interface
- Quad remote diode sensing
- Monitors 16 voltages
- Up to 12-bit (0.0625°C) resolution
- -127°C to +125°C temperature reading range
- 2 PWM fan control outputs, 6 temp. zones
- 4 Tachometer inputs
- Diode fault-detection



The LM94 is our latest hardware monitor and comes with our TruTherm capability for remote diode sensing which provides greater temperature accuracy with diodes of the newest small geometry products such as processors, graphics engines, large PLDs, and ASICs. Its ability to monitor 16 remote diodes, 16 separate voltages and 4 fans, together with its 2 fan-control outputs make it a very powerful device.

Furthermore, the wide temperature range capability and diode fault-detection capability further enhance its utility.

Hardware Monitor for Transmitter



**National
Semiconductor**
The Sight & Sound of Information

The LM94 is a very powerful hardware monitor, as indicated on the previous page. Here we see a simplified implementation in an RF transmitter application where remote temperatures and many voltages may be monitored and fans may be controlled. Communication with the host processor is through a two-wire SMBus.

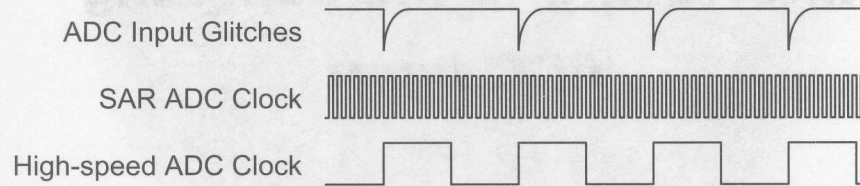
The 30 kΩ output impedance of the LMV227 may require that it be buffered to drive the LM94 input.

Interfacing to the Sampling ADC Input

The sampling ADC, unless the input is buffered, has analog input current pulses at the ADC sample rate. Let's take a look at how this affects the sampled signal and what should be done about it.

ADC Input Glitches – Passive Drive

- ADC input glitches are caused by sampling action
- It is not necessary to eliminate the glitches
- Input needs to settle before sampling switch opens



Sample switch closes on rise of clock,
causing input glitches

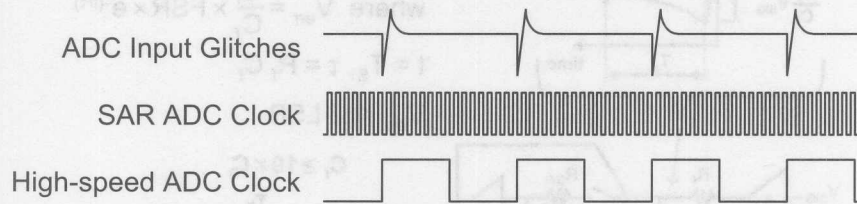


A look at the sampling ADC input will reveal pulses at the ADC sample rate. These pulses are caused by the recharging of the ADC sampling capacitor at the start of each conversion cycle. The user should not attempt to filter out these pulses, which are completely normal. However, the pulses should settle out before the end of the sampling time, which is generally specified in the datasheet.

In the case of high-speed ADCs with a sample rate equal to the ADC clock rate, the sampling time is usually either the clock low time (when the sampling edge is the rise of the ADC clock) or the clock high time (when the sampling edge is the fall of the ADC clock). ADCs based on Successive Approximation Register (SAR) usually sampled for more than one clock period.

ADC Input Glitches – Amplifier Drive

- ADC input glitches are caused by sampling action
- It is not necessary to eliminate the glitches
- Input needs to settle before sampling switch opens



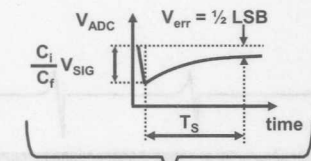
Sample switch closes on rise of clock,
causing input glitches



If a feedback amplifier (operational amplifier) is used to drive the ADC input, there may be overshoot as the amplifier over-corrects for the pulse. Again, there should be no attempt to filter out these pulses, but they should settle out before the end of the sampling time.

ADC Sampling Filter

- Input needs to settle before sampling switch opens
- Sampling filter isolates capacitance from amplifier while allowing input to settle

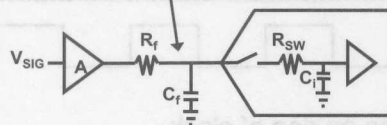


$$V_{ADC} = V_{SIG} - V_{err}$$

$$\text{where } V_{err} = \frac{C_i}{C_f} \times \text{FSR} \times e^{-(t/\tau)}$$

$$t = T_S, \tau = R_f C_f$$

$$V_{err} < \frac{1}{2} \text{LSB}$$



$$C_f \geq 10 \times C_i$$

$$R_f \leq \frac{T_S}{10 \times C_i \times \ln[10 \times 2^{-(n+1)}]}$$



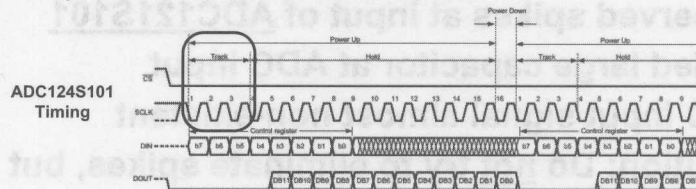
Standard practice when driving the input of sampling ADCs is to isolate the op amp output from the ADC input with a small resistor and a capacitor. The reason for this is to allow faster settling of the ADC input to ensure that it has settled before the ADC sampling switch opens. Additionally, some SAR ADCs can have a large input capacitance that might bring instability to the driving amplifier. The resistor between the amplifier output and the ADC input will isolate the ADC input capacitance from the amplifier output and improve loop stability of the amplifier.

For dynamic applications with AC signals up to half the sample rate, T_S should generally be the sampling time of the ADC, which can be found in the ADC datasheet.

Refer to the op amp datasheet for specific information when driving capacitive loads.

ADC Sampling Time from Datasheet

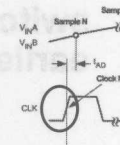
- The ADC124S101 timing diagram indicates 3 clock cycle track (sample) time
- The ADC12DL080 electrical table and the partial timing diagram tell us the sample time is the same as the clock low time.



Converter Electrical Characteristics (ADC12DL080)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DN} = +2.5V$, PD = 0V, External $V_{REF} = +1.0V$, $f_{CLK} = 80\text{ MHz}$, $f_{IN} = 40\text{ MHz}$, $C_L = 10\text{ pF}$ /pin, Duty Cycle Stabilizer On. Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_J = 25^\circ\text{C}$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	$V_{IN} = 1.5\text{ Vdc} \pm 0.5V$	(CLK LOW)	8	pF
			(CLK HIGH)	7	pF



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The ADC sampling time can be obtained from the datasheet timing diagram and, sometimes, from the electrical characteristics table.

The timing diagram of SAR-based ADCs will usually show the sampling, or track, time on the timing diagram, as indicated here for the ADC124S101, a 12-bit, 4-channel ADC specified for operation over the 500 kSPS to 1 MSPS range.

The data sheet electrical table for the ADC12DL080, a 12-bit, dual low power ADC specified at 80 MSPS, indicates that the sampling time is the time that that clock input is low. We know this because the input capacitance is highest during the sampling time. The timing diagram also indicates that the sampling time is the time that the input clock is low because the sampling period ends at the rise of the clock.

Customer Problem

- Application: “Black Box” cockpit voice recorder
- Observed spikes at input of ADC121S101
- Added large capacitor at ADC input
- ADC input signal almost non-existent
- Solution: Do not try to eliminate spikes, but allow spikes to settle out before sample switch opens (Use RC with f_c as described earlier)



This customer problem is a very common one. As mentioned before, the important thing is to allow the input to settle while the ADC sample switch is closed. The RC time constant should provide a pole as described on the previous slide.

Customer Problem: High Pitch “Whine”

- Application: “Black Box” cockpit voice recorder
- Using ADC121S021 at 44 kSPS
- High pitch “whine” in reconstructed recording
- Cause: Aircraft instrumentation (probably gyro) vibrated at a rate above the range of hearing that the microphone picked up and the ADC aliased
- Solution: Use an anti-aliasing filter



This customer problem was solved by adding an anti-aliasing filter. A 30 kHz vibration can not be heard directly, but when sampled at 44 kSPS, 30 kHz, for example, is aliased back to 14 kHz, which is audible.

Customer Problem: Rail-to-Rail Output Issue

- **Problem:** The output of a “rail-to-rail” amplifier may get down to 10 mV. With a 2.0V reference and an input range of 0V to 2.0V, how many LSB of a 10-bit ADC is this?

$$2V/2^{10} = 1.95 \text{ mV/LSB}$$

$$10 \text{ mV}/1.95 \text{ mV} = 5.12 \text{ LSB}$$

The lowest code, then, that will be seen at the ADC output is “5”.

- **Solution:** Use a pull-down resistor on the amplifier output



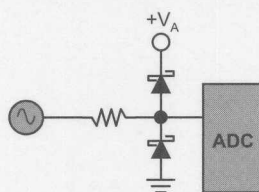
Rail-to-rail amplifiers are very nice products, but they do have their limitations. Here we see that, with a unipolar supply, a rail-to-rail output amplifier can not provide a signal swing that goes low enough to use the entire dynamic input range of the ADC. Of course, we lose more codes as the ADC resolution goes up.

If the full-scale input of the ADC is at the positive supply rail of the amplifier, we also will not see the codes near full-scale as well. On top of this, there is more distortion at the output of the amplifier as that output gets closer to the rails.

The solution for this customer was to use a pull-down resistor (270Ω) at the amplifier output. The resistor value will depend upon the type of amplifier used and how much distortion is allowed.

Input Overdrive

- Driving the ADC input beyond the supply rails can cause latch-up
- Potential problem when using different supplies for ADC and driving device
- Potential power-on or power-off problem
- Potential problem with power sequencing



Input Protection



If the input to any device, ADC or otherwise, is driven far enough beyond the supply rails for that device, the result can be a latch-up of that device. A hard latch-up can be destructive, but more often there is a soft latch-up whereby the device does not work properly or may not function at all.

Examples of potential problems include driving a single +5V supply ADC with an amplifier that is powered from $\pm 5V$, from $\pm 12V$ or +12V, or even from a separate +5V supply source from the ADC's power source.

Protecting the inputs with a resistor and two diodes, as shown here, is an effective way of protecting most ADC inputs. However, this may not be adequate for some devices, particularly some older devices.

The on-chip ESD diodes do not have a low enough forward drop to adequately protect against input overdrive.

Input Overdrive

- Driving the ADC input beyond the supply rails can cause latch-up
- Potential problem when using different supplies for ADC and driving device
- Potential power-on or power-off problem
- Potential problem with power sequencing



Input Protection

Microcontroller
VDDIO

If the input to any device, ADC or otherwise, is driven far enough beyond the supply rails for that device, the result can be a latch-up of that device. A hard latch-up can be destructive, but more often there is a soft latch-up whereby the device does not work properly or may not function at all.

A number of potential problems involving a single +5V supply ADC with an amplifier that is powered from a 5V, from a 12V or +12V, or even from a separate +3V supply source from the ADC's power source.

Protecting the inputs with a resistor and two diodes is always best, is an effective way of protecting most ADC inputs. However, this may not be adequate for some devices, particularly some video devices.

The on-chip ESD diodes do not have a low enough forward drop to adequately protect against input overdrive.

Noise Considerations

We know that noise is always an issue. Adding more circuitry usually adds more noise. There are things that can be done, however, to minimize the impact.

This is not what we generally expect to see in the way of a PSRR spec. A very careful look at the datasheet is usually required to see that the PSRR provided is what we have called DC PSRR and has absolutely nothing to do with how power supply noise is rejected from the output.

$$PSRR = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{0.001V}{0.01V} = 0.1$$

What is PSRR?

- Two different PSRR specifications
 - What you expect
 - What is on the data sheet
 - These two are usually NOT the same!
- DC PSRR – change in a DC parameter with change of supply voltage
- AC PSRR – How much supply noise gets through to the output
- Datasheets generally show DC PSRR



There are at least two different ways to specify Power Supply Rejection Ratio (PSRR). The PSRR spec we generally see on semiconductor datasheets is DC PSRR. That is, it tells us how much a certain parameter, such as offset error or gain, can be expected to change with a given change in the power supply voltage. For example, an ADC with a 5.5 mV offset error at a power supply voltage of 4.75V may have a 6.0 mV offset error at a power supply voltage of 5.25V, giving us a DC PSRR of

$$\text{PSRR} = -20 \times \log\left(\frac{\Delta \text{ offset Voltage}}{\Delta \text{ supply Voltage}}\right) = \left(\frac{0.006 - 0.0055}{5.25 - 4.75}\right) = \left(\frac{0.0005}{0.5}\right) = 60 \text{ dB}$$

This is not what we generally expect to see in the way of a PSRR spec. A very careful look at the datasheet is usually required to see that the PSRR specified is what we here call DC PSRR and has absolutely nothing to do with how power supply noise is rejected from the output.

Calculating AC PSRR

$$\text{AC PSRR} = 20 \times \text{LOG} \left(\frac{\text{Analog Supply Ripple}}{\text{Normalized Output Tone}} \right)$$

$$\text{Convert output noise from dB to Volts: Volts} = \sqrt{10^{\left(\frac{\text{dB}}{20}\right)}}$$

$$\text{Normalized Tone (NT)} = \text{Tone (dBFS)} + 20 \times \text{LOG} (\text{Ripple } V_{P-P} / V_{FS})$$

Ripple V_{P-P} = peak-peak power supply ripple

V_{FS} = peak-peak full scale input swing



AC PSRR, on the other hand, indicates how much noise on the power supply is rejected from the output.

To measure AC PSRR we look at the ADC output level of the power-supply noise frequency with a Frequency Domain (FFT) plot. Because the noise level on the power supply is generally lower than the full-scale input range of the ADC, we normalize the output noise level to what it would have been with a power-supply noise level equal to the ADC full-scale input range or swing. Because the result is a scalar, we convert it to dB. Then we add it (algebraically) to the (ripple) noise level. We negate that normalized figure and convert it to a voltage. The ratio of that result to the peak-to-peak ripple voltage is the AC PSRR.

Calculating AC PSRR Example

- Example: applying a 40 MHz, 200 mV_{p-p} signal to the supply pin of an ADC with a 2.0V reference results in a 40 MHz tone in the FFT plot at -63 dBFS. What is the PSRR at this 40 MHz?
- Solution:
 - Normalized Tone = -63 dB - 20 x Log(0.2/2.0)
= -63 dB - (-20)dB
= -43 dB
 - Tone in Volts = $10^{(-43/20)} = 0.007079V$
 - AC PSRR = 20 x Log(0.2/0.007079V) = 29 dB

This example illustrates the AC PSRR calculation process.

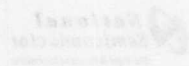


PSRR Question 1

A 10-bit ADC datasheet has a PSRR spec of 72 dB with “gain” listed as a condition. What does this mean? How much high-frequency noise can the ADC tolerate on the power supply?

“Gain” as a condition shows that PSRR indicates the sensitivity of gain to supply voltage variation

This kind of spec does not indicate the amount of noise that can be tolerated on the power supply



The condition of “gain” means that the specification is DC PSRR and is an indication of the effect that a change in the DC power supply voltage affects the ADC gain. This spec tells us nothing about the amount of noise that can be tolerated on the power supply.

PSRR Question 2

An ADC is being powered from a switching regulator with about 600 mV of ripple at 1 MHz. An FFT reveals a -66.4 dBFS spur at 1 MHz. The input dynamic range is 2V. What is the AC PSRR of this ADC at 1 MHz?

Since 600 mV is already about 10.5 dB below the 2V full scale range, the AC PSRR at 1 MHz is 10.5 dB worse than the 61 dB below full scale that we see at the output, or 55.9 dB

ADC Reference Influence

$$\text{Digital Output} = \text{INT} \left(\frac{V_{\text{IN}} \times 2^n}{\text{SF} \times V_{\text{REF}}} \right)$$

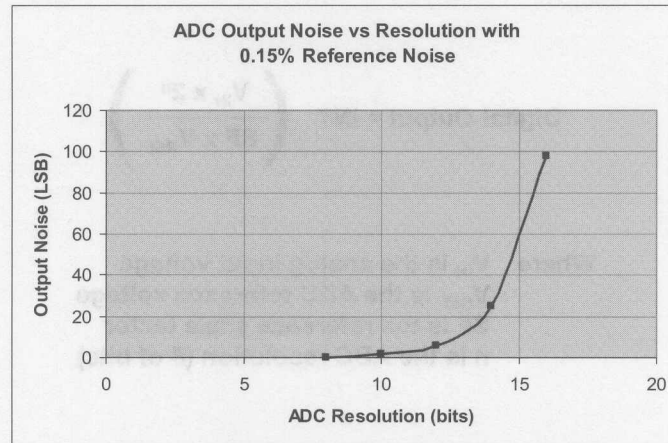
Where V_{IN} is the analog input voltage
 V_{REF} is the ADC reference voltage
SF is the reference scale factor
n is the ADC resolution (# of bits)



The ADC output tells us the ratio of the analog input voltage to the reference voltage. Because the digital output code is a function of the reference voltage, a change of the reference voltage will cause a change in the output code, just as does a change in the analog input voltage. Therefore, any noise or variation in the reference voltage appears at the ADC output.

The Scale Factor (SF) in the formula is something not usually discussed as it is most often unity. However, it is present and should be taken into consideration because some data converters have scale (gain) factors that are other than unity. The SF can be any number, whole or fractional.

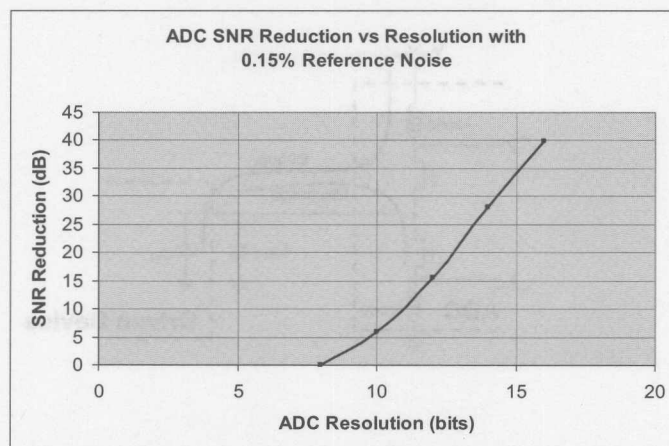
Reference Noise Effect vs Resolution



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This graph indicates the amount of output noise present with 0.15% noise on the reference voltage. Note that this amount of noise is tolerable at 8 bits and even seems tolerable at 10 bits, but the next page shows the amount of Signal-to-Noise Reduction (SNR) we have at this reference noise level.

Reference Noise and SNR Reduction vs Resolution

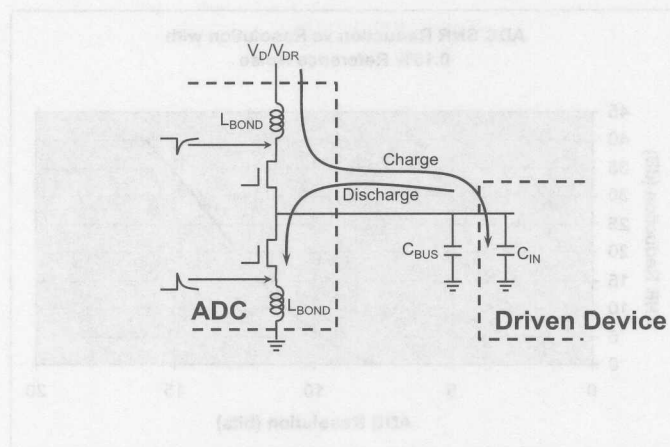


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The two LSB of peak-to-peak noise at 10 bits does not seem like much until you realize that it brings a 6 dB reduction in SNR performance. Of course, at higher resolutions the effect is much more dramatic.

If you calculate the amount of noise tolerable on the reference voltage needed for various resolutions, you will find that the tolerance is reduced by 50% for every additional bit of resolution. This means that the 0.1953% tolerance for $\frac{1}{2}$ LSB noise at 8 bits becomes 0.00076% at 16 bits and 0.00000298% at 24 bits. This points to the increasing importance of a quiet reference at higher resolutions.

High Capacitance on ADC Outputs



Since the well-bypassed supply line is isolated from the die by the bond wire inductance as an ADC output pin goes from low to high, we can have negative-going spikes on the supply line. We call this “ V_{CC} bounce.” If the supply line used for the output driver stage(s) is common with the supply line for other die areas, these spikes can couple into those areas. In the digital areas it can cause jitter-induced noise. In the analog areas it can directly add noise to the conversion process.

As the digital output(s) go from high to low, the charge on the bus and driven device input capacitances passes through the die substrate and the ADC ground pin. The ground bonding inductance isolates the die common from the nice, clean ground at the device pin and pulses of varying amplitude, depending upon how many outputs are discharged, occur on the die. We call this “ground bounce.” The die common, then, is not at ground or a steady voltage, but can vary enough to cause the difference between the input signal and ground to be noisy and we have a noisy conversion.

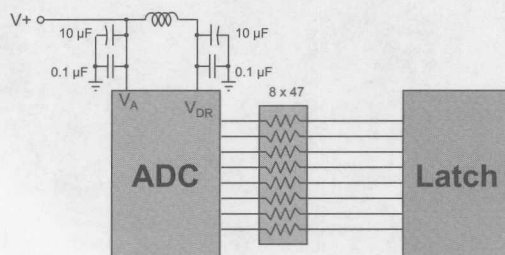
In the case of a differential input ADC, you would think that the Common Mode Rejection (CMR) of the differential input would eliminate the problem. However, the CMR of any circuit gets worse as frequency increases, typically getting rather poor as frequency exceeds a few hundred kilohertz. Since these ground-bounce pulses occur at rates up to the output data rate and since the fast rise time corresponds to even higher frequencies, the CMR at the frequencies involved is nearly zero.

The task, then, is to minimize these charge and discharge currents so that the induced noise is minimized.

The first step to minimizing this induced noise is to minimize the capacitive loading on the digital output pin(s). This means that a bus should not be directly driven by the ADC (thus the reason for a lack of newer ADCs having a tri-state output). Lower capacitance means less charge moved and less induced noise. So, it is important to drive only a single, low-capacitance input pin of a receiving device, which should be as close as possible to the ADC output pin(s).

Output to Input Coupling

- Output “talks” to input
 - Because of output capacitance
 - Through the supply
 - Through the substrate
- Limiting output current (with resistors) can help



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Sometimes, however, it is not possible to get the output capacitance low enough to eliminate the induced noise. This is especially true at higher ADC resolutions, low reference and signal levels, and higher sample rates. In this event it is helpful to use 47 to $100\ \Omega$ series resistors at the ADC output pins, located as close to the ADC output pins as possible. This limits the amount of current used to charge and discharge the capacitances on the ADC outputs and lowers the on-chip noise.

If the series resistors are not located very close to the ADC digital output pins, the board capacitance between the ADC and the resistors can be high enough to produce more noise than desired. This, again, is especially true at high resolutions, low reference and signal levels, and higher sample rates.

Offset Considerations

The cumulative offsets that are possible in the signal path is something that is not often considered. This can cause failures at the product test phase or in the field.

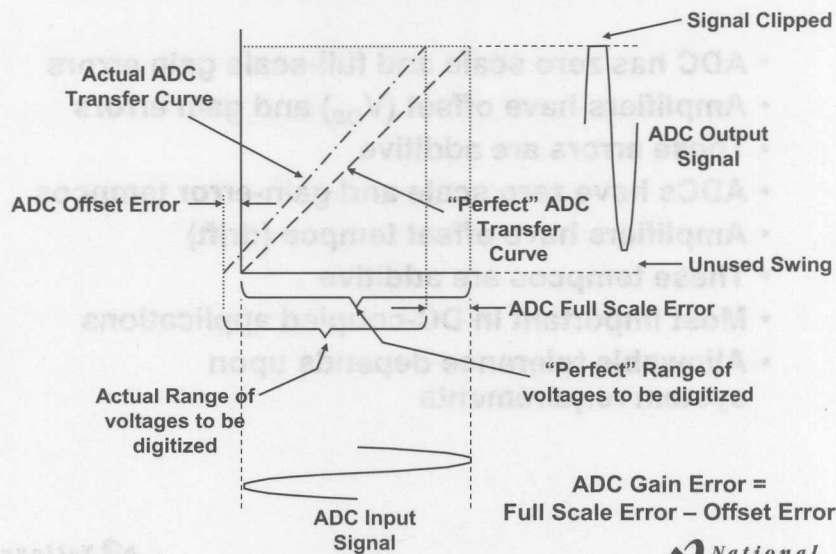
Be Aware of The Effects of Offsets

- ADC has zero scale and full-scale gain errors
- Amplifiers have offset (V_{OS}) and gain errors
- These errors are additive
- ADCs have zero scale and gain-error tempcos
- Amplifiers have offset tempco (drift)
- These tempcos are additive
- Most important in DC-coupled applications
- Allowable tolerance depends upon system requirements



Here we see some important considerations regarding offset and gain errors in the ADC and amplifiers that drive the ADC. How much of these errors can be tolerated is determined by system requirements.

ADC Offset and Gain Errors



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Offset and gain errors will affect the output unless we either allow for them or compensate for them. Of course, any amplifier offset error will add to the offset error of the ADC, as will any gain error.

Large V_{OS} Drift Reduces FSR

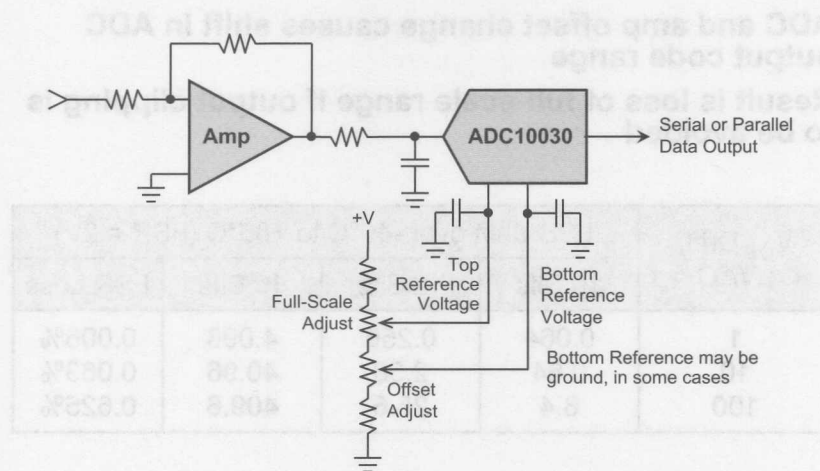
- ADC and amp offset change causes shift in ADC output code range
- Result is loss of full-scale range if output clipping is to be avoided

V_{OS} Drift, $\mu V/^{\circ}C$	LSB Shift over $-40^{\circ}C$ to $+85^{\circ}C$ (FSR = 2V)			
	10 Bits	12 Bits	16 Bits	FSR Loss
1	0.064	0.256	4.096	0.006%
10	0.64	2.56	40.96	0.063%
100	6.4	25.6	409.6	0.625%



If we are to avoid clipping of the ADC output, we must reduce the input swing to allow for worst-case offset and gain errors and their drifts. This means a loss of input dynamic range and a resulting loss of SNR performance.

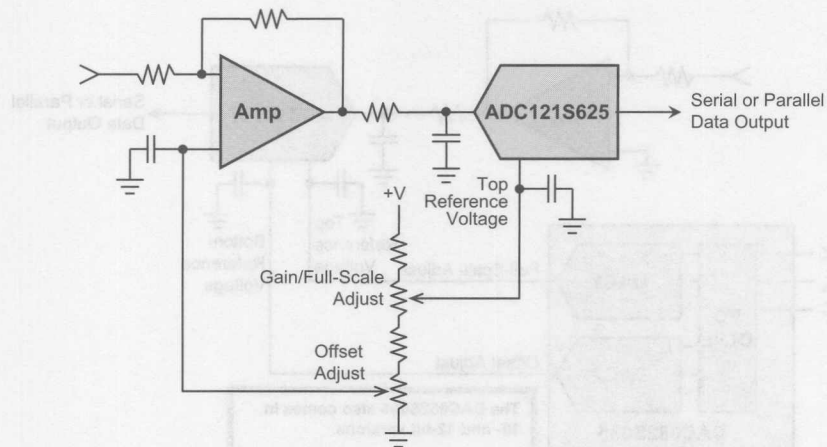
Manually Adjusted Offset and Gain Error Compensation



System gain and offset errors can be compensated for by slightly modifying the top and bottom reference voltages of the ADC. The problem here is that most ADCs have the bottom reference fixed to ground and cannot be adjusted. Furthermore, manufacturing people do not like manual adjustments, which are rather costly in production. As if this were not enough, offsets tend to have time and temperature drift.

Fortunately, there is a better solution for all of these cases.

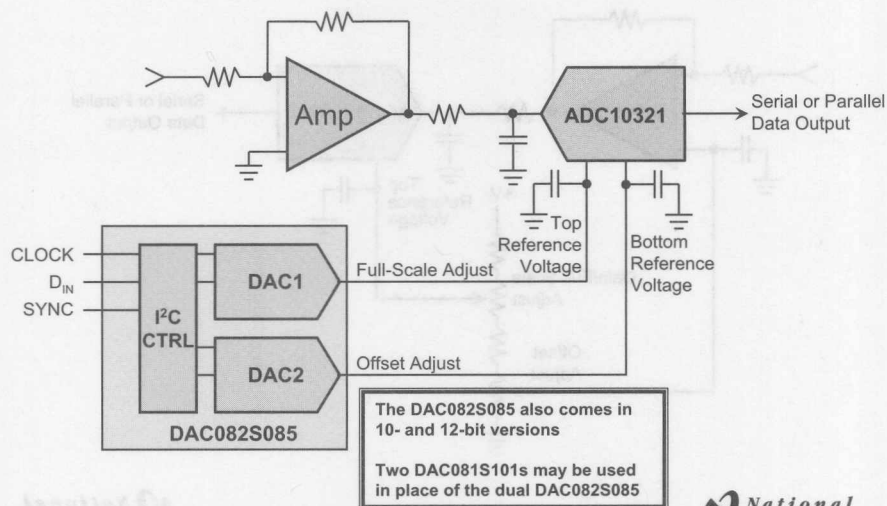
Manual Offset Adjustment Without Bottom Reference Access



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When the bottom reference of the ADC cannot be adjusted, the amplifier offset can be adjusted to null system offset errors. However, the problem with manual adjustments and drift are still present. But there is a way to get around this.

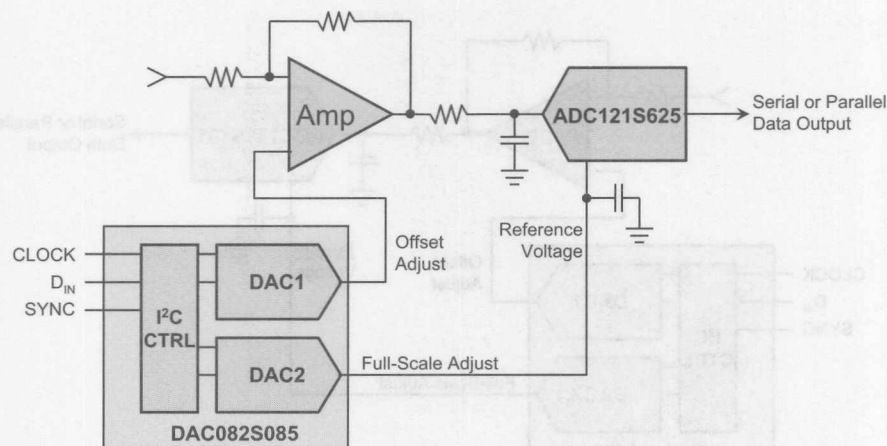
Processor Controlled Offset and Gain Error Compensation



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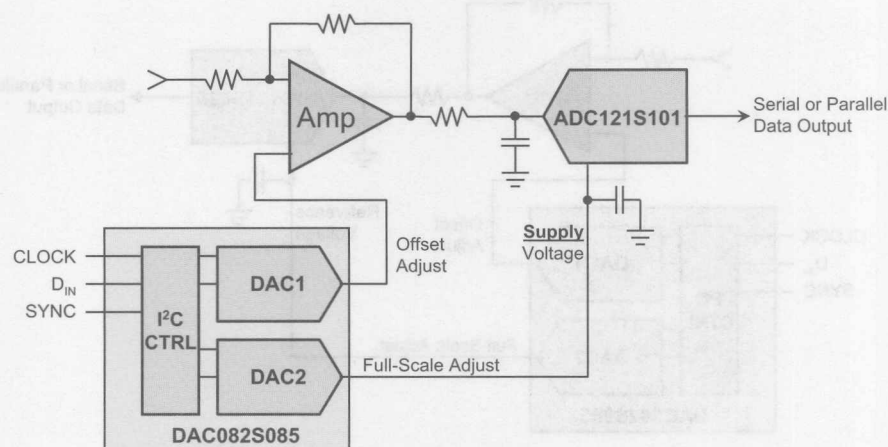
This solution has the advantages of processor-controlled adjustment of offset and gain errors whenever desired. For example, adjustments could be done upon application of power, when temperature changes by a preset amount (because of temperature drift) and when a preset amount of time has elapsed (because of time drift) since the last adjustment.

Processor Controlled Offset and Gain Error Compensation



If the bottom reference of the ADC cannot be modified, the offset adjustment can be done through the amplifier, as we saw with the manual adjustment.
Now, what can be done when the reference voltage is the supply?

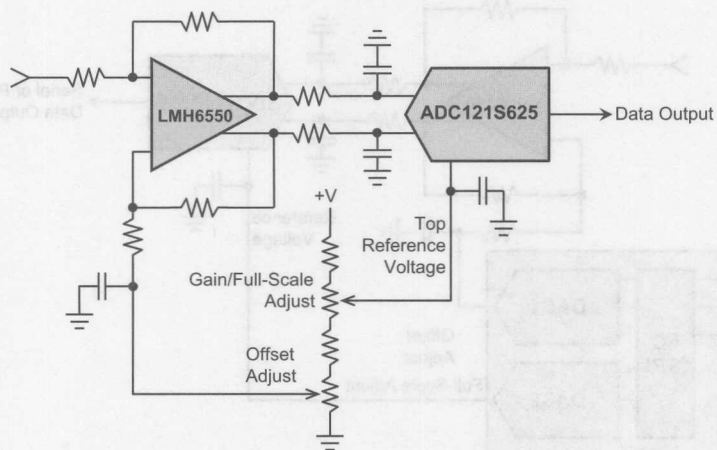
Automated Offset and Gain Error Compensation when Supply is Reference



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When the reference voltage is the supply voltage, such as is the case with National's ADC121S101, a DAC can be used to provide an adjustable supply voltage. Since the power consumption of our general-purpose ADCs is so low, driving the supply with a DAC is a simple matter.

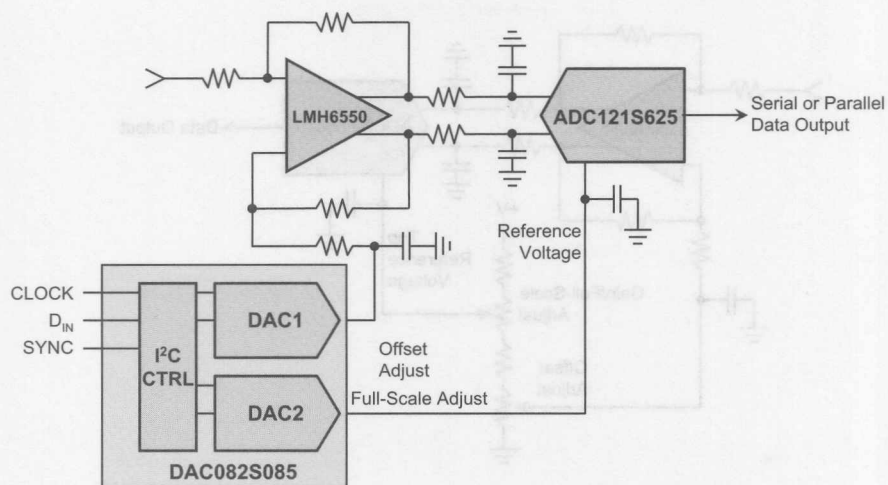
Manual Offset Adjustment Differential Input, No Bottom Reference Access



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Here is an example of full-scale and offset adjustment with a differential input ADC when the bottom reference voltage cannot be adjusted. This circuit shows the LMH6550, a fully differential amplifier, being used in a single-ended-to-differential conversion circuit.

Processor Controlled Offset and Gain Error Adjust, Differential Input



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Again, processor-controlled adjustment of the offset voltage is possible with a DAC in a circuit having a fully differential amplifier.

DAC Usage Considerations

- Quiet reference voltage or current
 - $V_{OUT} = V_{REF} \times G \times D/2^n$ (voltage output DACs)
 - $I_{OUT} = I_{REF} \times G \times D/2^n$ (current output DACs)
 - G = DAC gain factor
 - D = Digital input code
 - n = DAC resolution in bits
- When reference is supply
- Signal integrity



With any device, there often are considerations we do not think about. In the case of the DAC, we find that the importance of a quiet reference voltage is often overlooked, especially when the supply is the reference. Remember that since the output depends upon the reference, any noise on the reference will show up at the output, just as is the case with the ADC. When the reference voltage is the supply voltage, it is important to ensure that the supply voltage is very quiet. This often means using a separate regulator or reference source for the DAC supply line.

Of course, signal integrity is important to ensure that the expected information is loaded to the DAC.

General Purpose DACs

Features

- Guaranteed monotonicity
- Low-power operation
- Rail-to-rail voltage output
- SPI interface
- Reference is supply
- 2.7V to 5.5V supply
- Small packages
- Power down feature

Channels	Resolution		
	8-bit	10-bit	12-bit
1	DAC081S101	DAC101S101	DAC121S101
2	DAC082S085	DAC102S085	DAC122S085
4	DAC084S085	DAC104S085	DAC124S085

Drop-In
Replaceable
Across
Resolution
and Sample
Rate

National's new DACs are small, rail-to-rail output high performance DACs that address the most common DAC applications. We believe you will find these DACs to be among the best available.

Customer Problem: DAC121S101 Excessive Output Noise

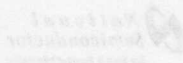
- **Problem:** Excessive noise on the DAC121S101 output
- **Conditions:**
 - DAC uses a 3.3V supply
 - Reference is the supply
 - Output reconstruction filter uses an LMV751 with a 5V supply
- **Discovered:** The 3.3V supply was the same used by 3V logic
- **Solution:** Use an LP2980 LDO with filtered 5V input for DAC121S101 supply



The customer did not think of the results of noise on the supply line when the reference is the supply. When this was brought to his attention, he immediately realized his error. The LP2980 Low Dropout (LDO) regulator did the job for this customer, but the LM4140 would provide a more accurate voltage for the sake of the reference. However, the closest voltages available are 2.5V and 4.096V. The LM4041 adjustable reference would be an excellent choice to obtain whatever voltage is required. The LM4041 is available with accuracies to 0.5%.

DAC121S101 Excessive Output Noise Customer Problem:

- Problem: Excessive noise on the DAC121S101 output
- Conditions:
 - DAC uses a 3.3V supply
 - Reference is the supply
 - Output reconstruction filter uses an LMV754 with a 5V supply
- Discovered: The 3.3V supply was the same used by 3V logic
- Solution: Use an LP2380 LDO with filtered 5V input for DAC121S101 supply



The customer did not think of the results of noise on the supply line when the reference is the supply. When this was brought to his attention, he immediately realized his error. The LP2380 Low Dropout (LDO) regulator did the job for this customer, but the LM4310 would provide a more accurate voltage for the sake of the reference. However, the closest voltage available was 2.5V and 4.0V. The LM43101 adjustable reference would be an excellent option to obtain whatever voltage is required. The LM43101 is available with accuracies to 0.5%.

Managing Jitter

Modern high-speed, high-resolution Analog-to-Digital Converters (ADCs) have very high resolutions and can accept and are used with input frequencies as high as hundreds of MHz and sometimes even beyond 1 GHz. Sensitivity to jitter increases with higher signal frequency and ADC resolution, so jitter management is an important consideration.

What is Jitter?

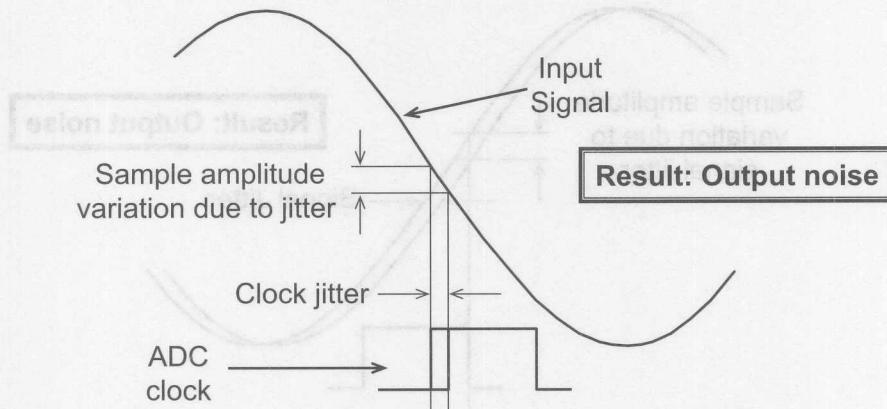
- Jitter – the cycle-to-cycle variation in the signal edge relative to another edge



Jitter is defined as the cycle-to-cycle variation in the edge of a signal and is usually spoken of as rms jitter.

Clock Jitter

Jitter: cycle-to-cycle variation in timing



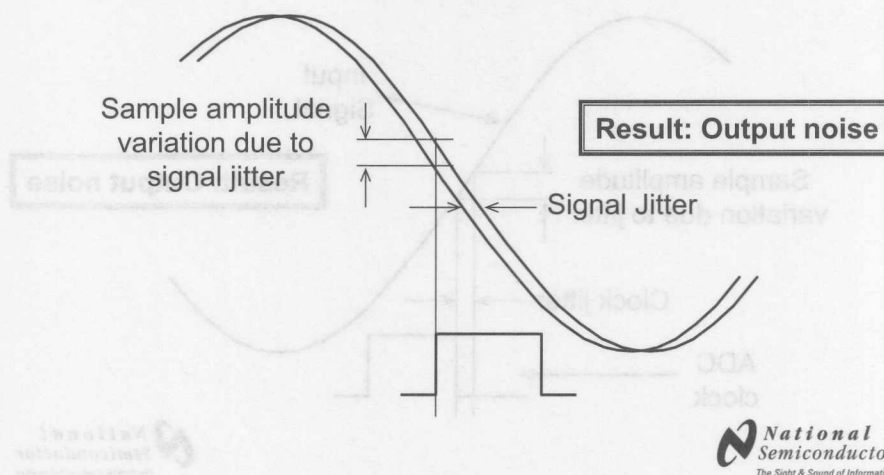
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Because jitter in the ADC clock relative to the input signal means that there is a variation in the time a signal is sampled, there is variation in the sampled signal level. If we try to sample the same point in a waveform at every cycle of that waveform, but there is jitter present, we may sample levels between, for example, 1.14V to 1.1V, or a 10 mV spread in this example. This means there is 10 mV of noise at the output. With 6- or 8-bit resolution, this might not be too bad. At higher resolutions, this can be significant.

The effect of jitter is more easily seen at higher resolutions (digital word widths) and higher frequencies.

Signal Jitter

Signal jitter has the same effect as clock jitter



When considering jitter in ADC applications, we generally think of clock jitter. However, jitter that is added by the circuitry to the input signal has the same effect as does jitter in the sample clock. The clock jitter relative to the signal jitter is where the problem exists.

High-Speed ADC Clock Considerations

- Maximum allowable jitter to prevent significant noise degradation:

$$t_{j,max} = \frac{V_{IN(P-P)}}{2^{(n+1)} \times V_{FS} \times \pi \times f_{in}}$$

- Clock rate has no effect upon jitter-induced noise



Jitter in the sampling clock or in the input waveform (actually, the jitter between the two) results in decreased noise performance, as we will see shortly. The maximum allowable jitter, from all sources, is as shown here if we are to prevent it from affecting performance. Jitter is a prime source of noise with digitized high-frequency signals. Note that sample rate does not enter this formula because, by itself, it does not affect sample placement. It is the input signal slew rate, which does not depend upon clock rate, that determines how much jitter affects the output signal.

Most people use a 2^n factor rather than the $2^{(n+1)}$ shown here, but that would limit the noise to one Least Significant Bit (LSB). Using a factor of $2^{(n+1)}$ limits the noise to $\frac{1}{2}$ LSB, which means, for all practical purposes, no jitter-induced noise.

High-Speed ADC Clock Considerations

- When the signal is a full-scale one, the formula reduces to:

$$t_{j,max} = \frac{1}{2^{(n+1)} \times \pi \times f_{in}}$$

Jitter and the Clock

- High-speed ADCs can exhibit jitter as low as 0.2 ps (rms). It is difficult to find clock sources with less jitter than about 1 ps (rms). For a system with a 12-bit ADC and with ADC input frequencies up to 25 MHz, is clock jitter a problem?

$$\begin{aligned}\text{Allowed } t_j &= 1/[2^{(n+1)} \pi f_{IN}] \\ &= 1/[2^{13} \pi 25 \times 10^6] \\ &= 1.55 \text{ ps}\end{aligned}$$

ADC + External Clock Jitter = 1.2 ps,
which is less than the 1.55 ps allowed.
No problem at 12-bits, 25 MHz.



Knowing how much jitter your ADC can tolerate without affecting its performance is important. After you know how much can be tolerated, you must find a clock source with sufficiently low jitter so that this rms jitter, plus the rms jitter added to the signal by the circuitry and the rms jitter of the ADC itself, added in an RSS manner, is less than the tolerable amount.

Jitter and the Clock

- The ADC12L080 is a candidate for a narrow-band 78 MSPS application with an input frequency of 148 MHz. The data sheet indicates an rms jitter of 0.7 ps. The ADC required resolution is just 8 bits (12-bit ADC used for input dynamic range) and the ADC will be operated with an input signal level of -24 dBFS. The jitter of the clock source is specified at 2 ps rms. Will clock jitter be a problem in this application?

8-bit performance required, so "n" = 8

$$\begin{aligned}\text{Allowed } t_j &= 1/[2(n+1) \pi f_{IN}] \\ &= 1/[2^9 \pi 148 \times 10^6] \\ &= 4.2 \text{ ps}\end{aligned}$$

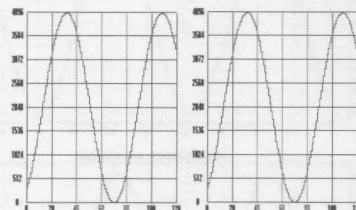
ADC + External clock jitter = 2.7 ps, which
is less than the 4.2 ps allowed

There is no problem for this application

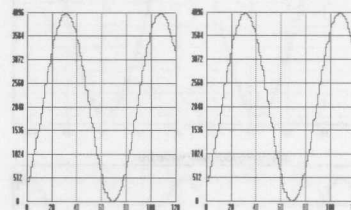


This example illustrates how we determine if the jitter of a specific ADC is adequate for the application.

Effects of Jitter – 1



Sampled with “clean” Clock



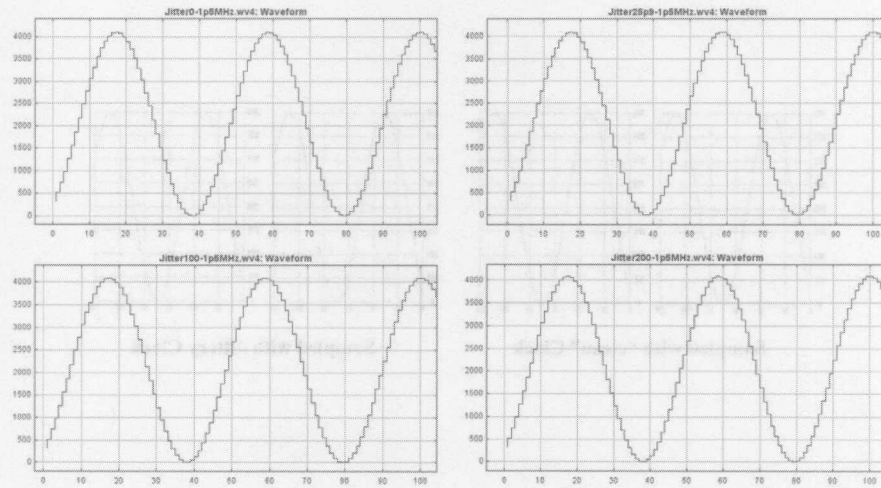
Sampled with Jittery Clock

WaveVision2
National Semiconductor

National
Semiconductor
The Sight & Sound of Information

These plots from National's WaveVision2 software show the effects of excessive clock jitter. The noise on the signal is apparent. Normally, you would never see the noise from clock jitter on a time domain plot. We had to force enough jitter to demonstrate this much noise.

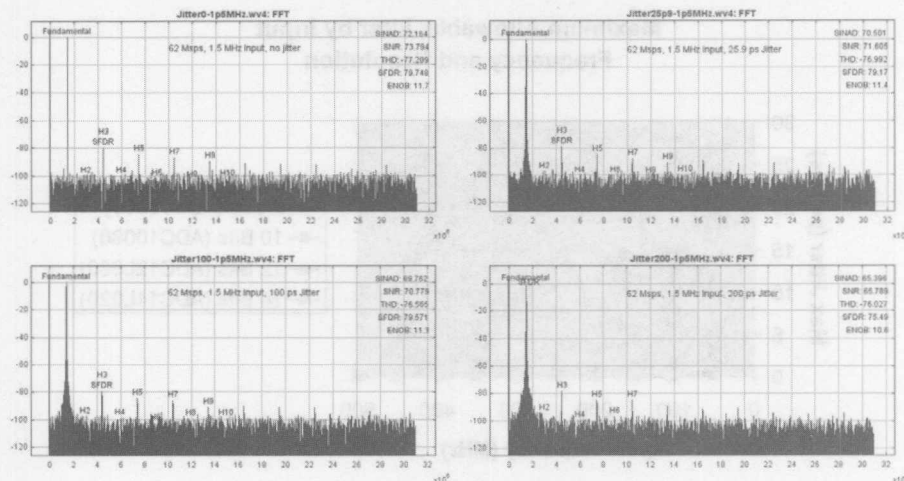
Effects of Jitter – 2



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All of these wave forms (taken with National's WaveVision4 software) look pretty much the same, yet they were captured with varying amounts of jitter in the sample clock. We need to look at a frequency domain plot to see the difference.

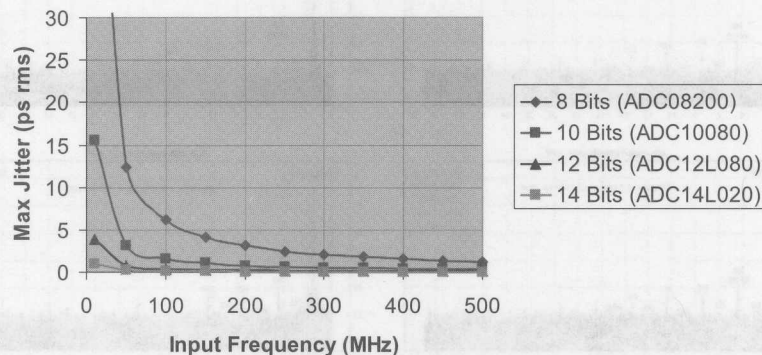
The Frequency Domain Plot and Jitter-Induced Noise



With frequency domain plots, we can easily see the effects of jitter. The top left plot is taken with no significant clock jitter. The top right plot is taken with 25.9 ps (rms) of jitter, which is, according to our formula, the maximum allowable jitter. Note that we see about a 2 dB degradation in Signal-to-Noise Ratio (SNR) and Signal-to-Noise And Distortion (SINAD) with this amount of jitter. Note also the spectral leakage, or “spreading,” of energy around the base of the fundamental. The reason for the degradation is because we did not allow for the jitter in the ADC itself or for any jitter in the input signal. If the total jitter in all of these sources were 25.9 ps (rms) or less, we should see very little difference in the top two plots. The other plots show the effects of higher amounts of jitter.

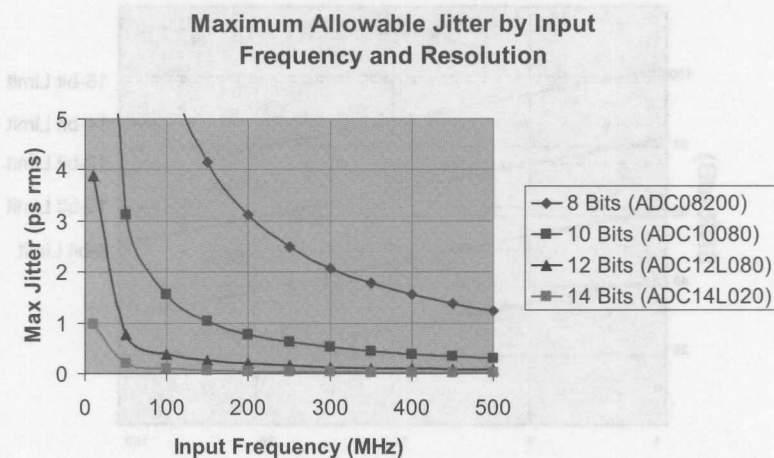
Maximum Jitter

Maximum Allowable Jitter by Input Frequency and Resolution



The maximum jitter tolerable without suffering a degradation in SNR is determined by the resolution of the ADC and the frequency of the input signal, as well as the signal amplitude relative to full scale. The curves are for a full-scale input signal to the ADC. Again, the sample rate has no effect upon the maximum allowable jitter to prevent noise degradation.

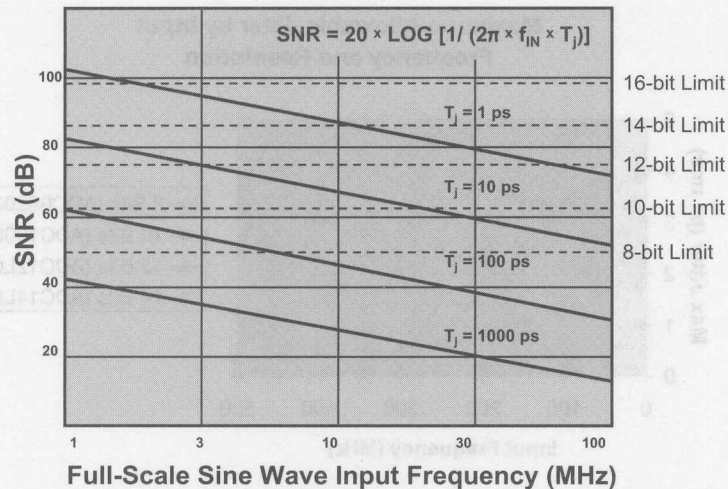
Maximum Jitter(2)



This is the same as the previous slide with the vertical scale expanded.

It seems that avoiding noise-induced jitter is an impossible task at very high input frequencies or at high resolutions. Careful selection to the the clock source and how it is presented to the ADC, as well as proper attention to design and layout, will go a long way toward maximizing circuit performance.

Jitter Effect Upon SNR



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This graph shows the relationship between ADC input frequency, SNR, and clock jitter. Of course, SNR will never be better than that indicated by the ADC resolution. Best $SNR = (6.02n + 1.76)$ dB, where “n” is the ADC resolution. Therefore, the best theoretical SNR for an 8-bit ADC is about 49.9 dB and the best theoretical SNR for a 16-bit ADC is about 98.1 dB. The theoretical SNR limit by resolution is shown with the dashed lines here.

Minimizing Jitter

- Decouple ADC input from the driving amplifier
- Minimize effect of output capacitance
- Use controlled impedance signal and ADC clock lines
- Minimize components in the signal and clock paths
- Any logic in clock path needs fast rise time
 - A related rule of thumb is that Logic's toggle capability should be at least 5 times the logic f_{IN}
- Use a low-phase noise clock source (e.g., a crystal-based clock)
- Do NOT use a clock signal from an ASIC, FPGA or microcontroller
- Use a clock divider
- Keep supply of analog input and clock driving circuits as noise-free as possible
- Avoid overloading clock source



Full attention to these guidelines will help minimize noise problems.

Using a controlled impedance clock line implies one source driving a single destination.

Logic components tend to add jitter to the signal unless their toggle capability is significantly higher than the actual toggle rate.

ASICs, FPGAs, and microcontrollers will generally add phase noise (jitter) to a signal. If the ADC input frequency is in the MHz range, it is generally better to not supply the ADC clock from these devices.

Starting with a high-frequency clock and dividing it down (using circuitry capable of toggle rates much higher than the starting frequency) will reduce clock jitter, if done properly.

If the supply of the circuits used to drive the ADC clock or the ADC analog input is not fairly free of noise, these circuits can often add significant jitter to the signal.

Overloading a clock source can add a lot of jitter to the clock signal. A high capacitive load on a crystal-based overtone oscillator can cause it to operate in its fundamental mode rather than its intended overtone mode.

Signal Integrity and PCB Layout Considerations

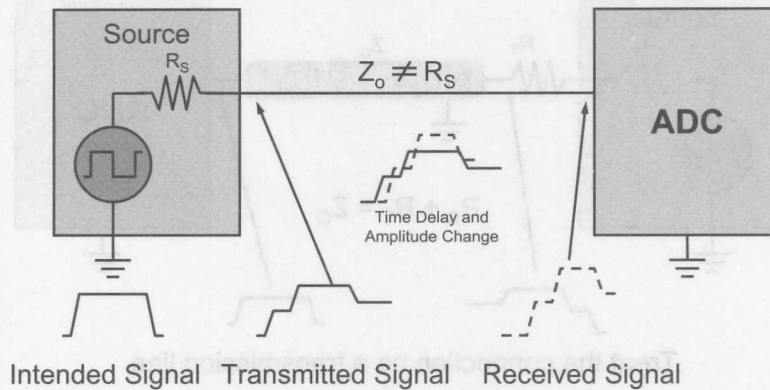
Signal integrity has become a popular topic in light of the very high edge rates that have resulted from today's technology. Working with today's high-speed digital signals has meant that digital designers must be concerned with signal integrity. Signals associated with modern data converters are no exception.

Actually, even modern, lower-speed converters can be affected because digital circuitry today, even with low toggle rates, tends to have very fast edge rates (rise and fall times). It is these edge rates that require attention to signal integrity, not just the toggle rate.

Layout considerations take us into what might be a whole new world - a "Twilight Zone", if you will - and are very much concerned with signal integrity. We will try to simplify these considerations and give you a couple of examples of typical problems in this area.

Signal Integrity Problem

This is NOT a controlled impedance line



Transmitted
Signal

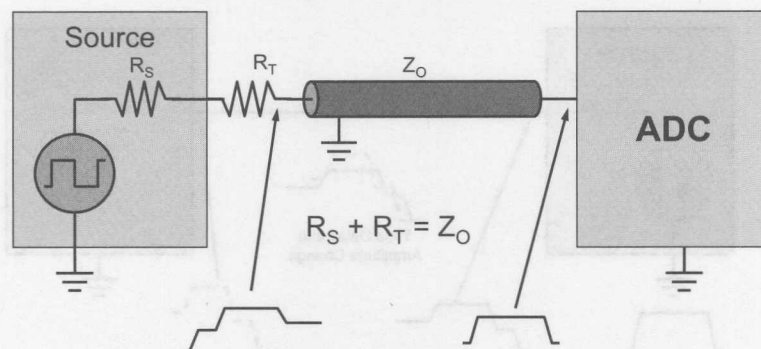
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All interconnecting lines are transmission lines. If the transmission-line characteristic impedance (Z_0) is not matched to the signal-source impedance (R_s) or the signal-receiver input impedance, there will be reflections on the line that can cause distortion and even an amplitude change (increase or decrease) of the signal. This loss of signal integrity could cause any number of problems in a system.

In the case of the data converter clock line, this mismatch can result in noise, missing codes, erratic operation, or even a complete malfunction.

Maintaining Signal Integrity

This IS a controlled impedance line



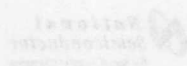
Treat the connection as a transmission line



Adding a series terminating resistor such that its value plus the signal-source impedance equals the characteristic impedance of the transmission line will usually ensure the integrity of the signal at the far (receiving) end and prevent problems, even without far-end termination. R_T should be as close as possible to the signal source.

Signal Traces vs Transmission Line

- “Long” lines are not simply traces
- Transmission lines can distort signals
- Distorted digital signals produce:
 - Timing uncertainty
 - Clock or signal jitter
- Through-hole problem
- Layout can be critical



Here is a brief review of some important points we have covered:

All signal-carrying lines are transmission lines. Beyond a certain length we absolutely must treat them as such if we are to avoid signal distortion, timing problems, and jitter.

Through-holes in a transmission line create impedance discontinuities and cause reflections with their attendant distortion and noise problems. A through-hole in a PCB has about 1 to 1½ nH of inductance, which can create problems. For example, a 14-bit, 80 MSPS ADC must have pins. bypass capacitors that are no more than 2 to 3 mm from the bypassed Putting these capacitors on the opposite side of the board results in the capacitors being isolated from the ADC by the ¼ to ¾Ω (at 80 MHz) of the through-hole inductance plus another ¼ Ω or so in the trace inductance.

Layout is critical for transmission lines, as these can experience impedance discontinuities when other lines approach them and depart from them. This is true even of the return current paths in the ground plane.

Maximum Trace Length

All traces are transmission lines, but a trace length longer than this absolutely must be treated as a transmission line:

$$L_{MAX} = \frac{t_R}{6 \times t_{PD}}$$

where L_{MAX} is the maximum line length beyond which that line must be considered a transmission line

t_R is the signal rise time

t_{PD} is the signal propagation rate down the board

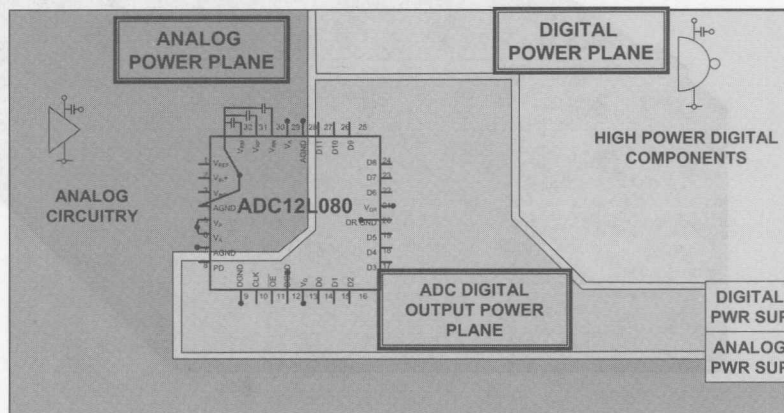


We have shown that a PCB trace can become a transmission line at a surprisingly short distance. Digital rise time (NOT repetition rate or frequency) is what we use to determine maximum trace length before it must be considered a transmission line. For analog signals, we can use 30% of the period of the highest frequency component, divided by its peak-to-peak amplitude, in place of rise time.

Recommended ADC Layout Example

Use a Single, Solid Ground Plane

• Black dots are vias to appropriate PWR or GND plane



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This recommended ADC layout will allow the best performance that the ADC can offer. To summarize the requirements:

Use a solid, unified ground plane. DO NOT split the ground plane. If there are ground planes in more than one board layer, connect them all together with a grid of through-holes (vias) on a spacing of about 1" or less.

Split the power plane, keeping each power plane in the same board layer. There should be separate power planes for (1) analog circuitry, (2) digital circuitry, and (3) the ADC digital output drivers.

Use analog power for the ADC digital core supply, but NOT for the ADC digital output drivers.

The power for the ADC digital output drivers may be the same supply as for the component(s) driven by the ADC outputs.

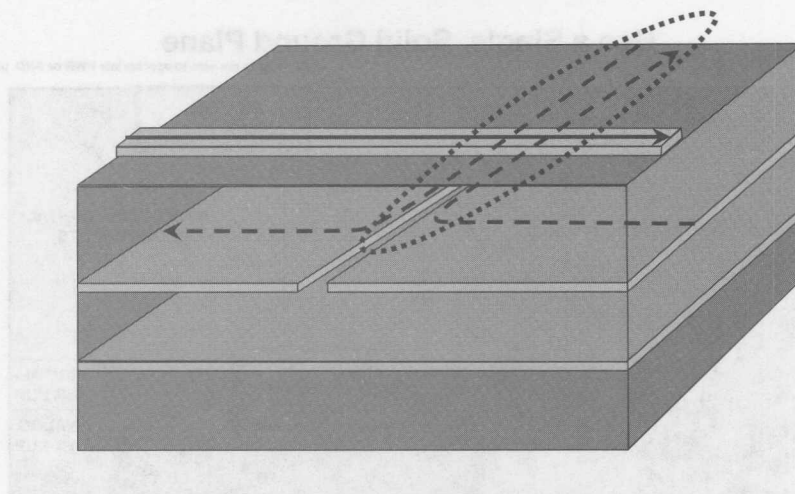
Locate all analog components and lines over the analog power plane and all digital components and lines over the digital power plane.

Use separate power sources for each plane. The ADC digital-output power can come from either power source, but should be decoupled with a series choke. It is generally best to use a linear voltage regulator for the ADC analog power source.

If any digital circuitry is powered by the same supply as the ADC output drivers and has signal lines going to the other digital area of the board, use capacitors between the two power planes. Locate these capacitors very close to the signal lines. This is discussed in the next few pages.

The ADC12L080 example shown here is a low-power 12-bit, 80 MSPS ADC intended for wireless communication applications.

When A Trace Crosses A Plane Boundary



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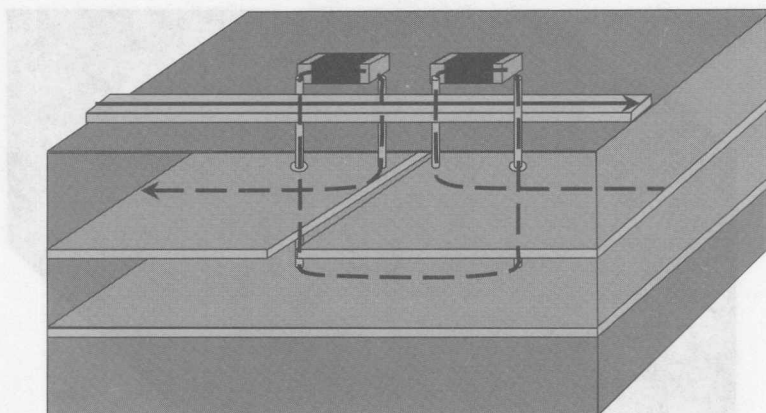
The plane in which return current flows is not always the ground plane. Current will follow the path of least impedance, and the least impedance path is the one where magnetic field fringing is the least (proximity effect). This, in turn, is where the outgoing and return currents remain as close to each other as possible. By design, the power delivery system is a low impedance one, so provides a low impedance path. If the power plane is closer to the outgoing path than is the ground plane, the return current will flow in the power plane.

If the outgoing current path crosses a boundary between two power planes, then the current must go around the break and find a path to the other power plane. This may be through the power supply, which might be a very long distance away. The loop area thus formed is very large and forms an antenna that can both radiate and pick up energy, possibly requiring shielding that would otherwise not be necessary.

Another problem occurs when this path deviation causes the return currents to flow coincident with other AC (return) currents (power planes tend to have a lot of AC currents). This common current path causes crosstalk that can result in noisy analog signals and can cause timing errors and jitter in digital signals.

BOTTOM LINE: Avoid having lines cross any plane boundaries whenever possible.

Capacitors Shorten the Return Path

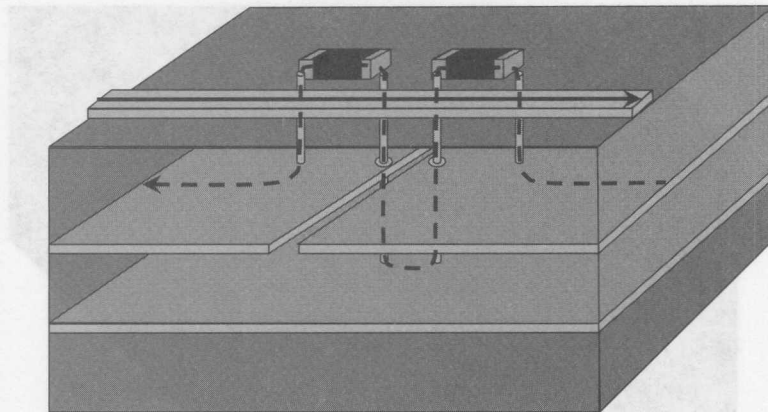


Sometimes it is necessary to have lines cross a plane boundary. When this is the case, add two capacitors right near the plane boundary to shorten the return current path.

Use of a single capacitor between the two planes is not desired, as this couples noise from one plane into the other. Less noise is coupled with two individual capacitors to ground.

A careful look at the return current path reveals that, although the path is shorter than it would be without these capacitors, there is a looping of current that can make up a small inductance, increasing the impedance of the path in this area.

Proper Via Placement Lowers Return Path Impedance



If we exchange the via placement such that the two vias nearest the plane boundary go to the more distant plane, the current path is a shorter one with less impedance.

The reason for not putting a single capacitor between the two power planes is to avoid the noise on one plane from being coupled to the other plane.

Summary of Layout Rules

- **Use a single, unified ground plane**
- **Split power planes**
- **Let trace routing control ground currents**
- **Try to avoid traces crossing plane boundaries**
- **Use capacitors when crossing plane boundaries is necessary**
- **Tie down grounded copper areas at many points**
- **Remember: Traces are transmission lines**



Here is a summary of rules for maximizing data converter and mixed-signal performance. While originally intended for high-speed circuits, we find that these guidelines are just as applicable for lower-speed circuits because of the fast digital edge rates we have today. It is these edge rates, not so much frequency, that determine circuit and layout needs.

All signal carrying lines are transmission lines. Beyond a certain length, we absolutely must treat them as such if we are to avoid signal distortion, timing problems, and jitter.

Through-holes in a transmission line create impedance discontinuities and cause reflections with the distortion and noise problems that come with reflections. A through-hole in a PCB has about 1 to 1½ nH of inductance, which can create problems.

Layout is critical for transmission lines, since they can experience impedance discontinuities and reflections when other lines approach them and/or depart from them. This is also true of the return current paths in the ground plane.

Much of this takes us back to what some of us learned in school but never used.

Specific Products and Application Examples

While this section of the seminar has focused mainly on the successful use of Analog-to-Digital Converters (ADCs), what follows is a brief summary of the characteristics of some of our ADC product types and some specific applications.

National's Data Converters



Highest Performance at the Lowest Power Consumption

8-/10-/12-/14-bit cores
ADCs, DACs
General-purpose family
High-speed family
Gigahertz family

Leading supplier in many applications

Communications
Ultrasound
Digital TV
Instrumentation
Imaging
Portable systems
Control systems
Etc.



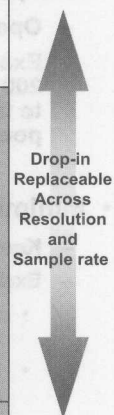
We take pride in the high performance of our data converter products and the fact that we can provide such products, often at lower power. Our product offerings are in resolutions between 8 and 14 bits and application space includes virtually all commercial areas.

New General-Purpose ADC Family

8-/10-/12-Bit Resolution

SPI Interface, Single-Ended Input

Res	Sample Rate	Channels			
		1	2	4	8
8 bit	50 to 200 kSPS	ADC081S021	ADC082S021	ADC084S021	ADC088S022
	200 to 500 kSPS	ADC081S051	ADC082S051	ADC084S051	ADC088S052
	500 kSPS to 1 MSPS	ADC081S101	ADC082S101	ADC084S101	ADC088S102
10 bit	50 to 200 kSPS	ADC101S021	ADC102S021	ADC104S021	ADC108S022
	200 to 500 kSPS	ADC101S051	ADC102S051	ADC104S051	ADC108S052
	500 kSPS to 1 MSPS	ADC101S101	ADC102S101	ADC104S101	ADC108S102
12 bit	50 to 200 kSPS	ADC121S021	ADC122S021	ADC124S021	ADC128S022
	200 to 500 kSPS	ADC121S051	ADC122S051	ADC124S051	ADC128S052
	500 kSPS to 1 MSPS	ADC121S101	ADC122S101	ADC124S101	ADC128S102
Package		SOT-23-, LLP-6	MSOP-8	MSOP-10	TSSOP-16



National's first new family of General-Purpose (GP) ADCs are drop-in replaceable across resolution and sample rate and have the same pinout and input impedance. All of these ADCs have single-ended inputs, use the supply as a reference, and have an SPI interface. All of these multi-channel parts have multiplexed inputs.

Applications Using Power-Down

- Sample rates below 50 kSPS
 - Operate at desired sample rate using \overline{CS}
 - Example: The ADC121S021 (guaranteed from 50 kSPS to 200 kSPS) can be used in a 5 kSPS application by running clock to the ADCs at 1 MHz (50 kSPS sample rate) with the ADC in power-down 90% of the time
- Minimizing power consumption
 - Keep the ADC in power-down as long as possible
 - Example: Using the ADC121S101 for a 500 kSPS application –
 - Run clock at 10 MHz (500 kSPS sample rate) without using power-down and consume rated power
 - Run clock at 20 MHz (1 MSPS sample rate) with the ADC put into power down 50% of the time, reducing the power consumption by almost 50%



The power-down mode allows operation at user desired sample rate while the ADC is run at maximum clock rate, resulting in a reduction of average power consumption.

To determine power consumption, multiply the active power consumption by the percentage of time in the active mode and add to this the product of the power-down power consumption and the percentage of time in the power-down mode.

Three Standard Speed Ranges, Three Resolutions

National Offers Guaranteed Performance Over a Range of Speeds!

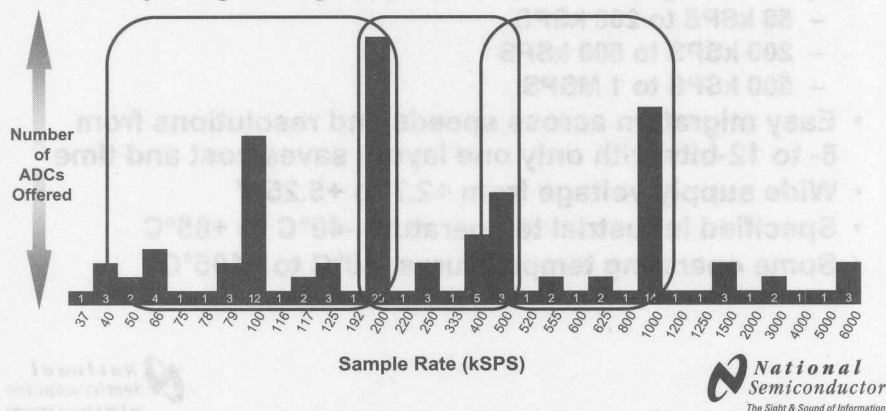
- **Speed Ranges:**
 - 50 kSPS to 200 kSPS
 - 200 kSPS to 500 kSPS
 - 500 kSPS to 1 MSPS
- **Easy migration across speeds and resolutions from 8- to 12-bits with only one layout saves cost and time**
- **Wide supply voltage from +2.7 to +5.25 V**
- **Specified industrial temperature -40°C to +85°C**
- **Some operating temperatures -40°C to +105°C**



National's family of general-purpose ADCs are guaranteed across a range of speeds. This is unique in the industry. Conventional ADCs are guaranteed at only one speed, so it can take five or six competitive devices to cover the same range of speeds National covers with a single product. Customers who use a variety of conventional general-purpose ADCs can usually standardize on just a few National ADCs.

ADI, TI, Maxim 12-bit Product Offering by Sample Rate (across all channels)

- Competitors need many products to cover GP sample rates
- We cover most sample rates with 3 products
 - National GPADCs are interchangeable with other ADCs of the same package configuration



Competitors need many products to cover general-purpose applications and have brought out their products over time by making incremental additions to their product line. Each of their devices is guaranteed at only one sample rate.

National's ADCs are guaranteed over a range of sample rates, which is unique in the industry. We have a standard pin-out for each channel configuration, and ADCs of the same package configuration are interchangeable across resolution and sample rates. This also is unique in the industry and allows our customers to easily migrate to new ADCs as sample rate and resolutions requirements change.

Guaranteed Performance Over Resolution, Channels, and Sample Rate

- Three standard sample rate ranges for each resolution and sample rate – **Performance Guaranteed**
 - 500 kSPS to 1 MSPS
 - 200 to 500 kSPS
 - 50 to 200 kSPS
 - < 50 kSPS (use power-down to get any lower sample rate – see notes)
- Each addresses 2 to 3 times as many competitive units

**** Major Difference from Competitors ****



National's new ADCs are guaranteed over one of three standard sample rate ranges. This means that you get guaranteed performance where you actually use the product.

National's ADCs replace several competitive units, and a power-down feature can be used to address sample rates down to essentially zero and to minimize power consumption.

Typical Competitive Guarantee

Competitors only guarantee performance at a single sample rate

AD7476—SPECIFICATIONS

(A Version: $V_{DD} = 2.7$ V to 5.25 V, $f_{CLK} = 20$ MHz, $f_{SAMPLE} = 1$ MSPS unless otherwise noted; S and B Versions: $V_{DD} = 2.35$ V to 5.25 V, $f_{CLK} = 12$ MHz, $f_{SAMPLE} = 600$ kSPS unless otherwise noted; $T_A = T_{HS}$ to T_{HSD} unless otherwise noted.)

Parameter	A Version ^{1,2}	B Version ^{1,2}	S Version ^{1,2}	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal-to-(Noise + Distortion) (SINAD) ³	69	70	69	dB min	$f_{IN} = 100$ kHz Sine Wave B Version, $V_{DD} = 2.4$ V to 5.25 V $T_A = 25^\circ\text{C}$
	70		70	dB min	
Signal-to-Noise Ratio (SNR) ³		71.5		dB typ	
	70	71	70	dB min	B Version, $V_{DD} = 2.4$ V to 5.25 V
		72.5		dB typ	
Total Harmonic Distortion (THD) ³	-80	-78	-78	dB min	
Peak Harmonic or Spurious Noise (SFDR) ³	-82	-80	-80	dB typ	
Intermodulation Distortion (IMD) ³				dB typ	
Second-Order Terms	-78	-78	-78	dB typ	$f_a = 103.5$ kHz, $f_b = 113.5$ kHz
Third-Order Terms	-78	-78	-78	dB typ	$f_a = 103.5$ kHz, $f_b = 113.5$ kHz
Aperture Delay	10	10	10	ns typ	
Aperture Jitter	30	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY					
Resolution	12	12	12	Bits	S, B Versions, $V_{DD} = (2.35$ V to 3.6 V) ⁴ ; A Version, $V_{DD} = (2.7$ V to 3.6 V)
Integral Nonlinearity ³	± 1	± 0.5	± 1.5	LSB max	
		± 0.6	± 0.6	LSB typ	

- A Version specified at 1 MSPS, B and S versions at 600 kSPS



This is one of a competitor's leading 12-bit ADCs. It is a fine product with performance guaranteed over supply voltage and temperature. However, there are three versions, each with its own advantages and only guaranteed at one sample rate.

National's New GPADC Specification

New GPADC family is guaranteed over a range of sample rates

ADC121S101 Converter Electrical Characteristics

The following specifications apply for $V_{DD} = +2.7V$ to $5.25V$, $f_{SCLK} = 10$ MHz to 20 MHz, $f_{SAMPLE} \leq 500$ kSPS to 1 MSPS unless otherwise noted. Boldface limits apply for $T_A = -40^\circ C$ to $+85^\circ C$; all other limits $T_A = 25^\circ C$, unless otherwise noted.

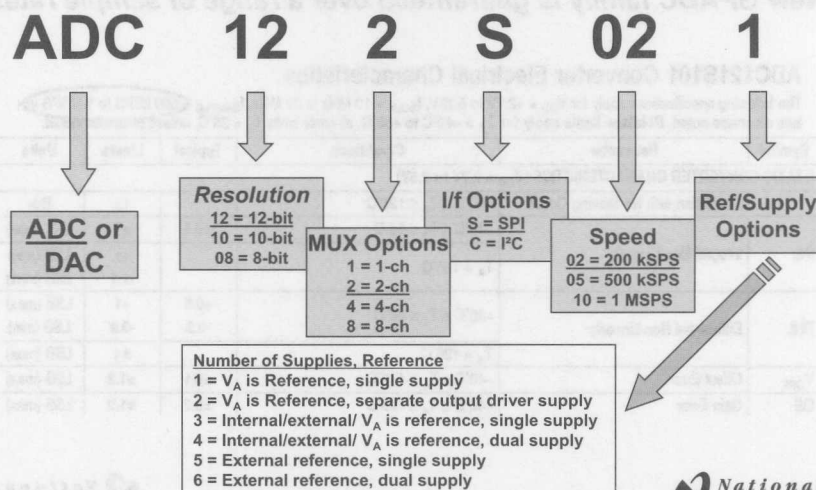
Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS ($V_{DD} = 2.7V$ to $3.6V$)					
	Resolution with No Missing Codes	$-40^\circ C \leq T_A \leq 125^\circ C$		12	Bits
INL	Integral Non-Linearity	$-40^\circ C \leq T_A \leq 85^\circ C$	± 0.4	± 1	LSB (max)
		$T_A = 125^\circ C$		+1	LSB (min)
				-1.1	LSB (max)
DNL	Differential Non-Linearity	$-40^\circ C \leq T_A \leq 85^\circ C$	+0.5 -0.3	+1	LSB (max)
		$T_A = 125^\circ C$		-0.9	LSB (min)
				± 1	LSB (max)
V_{OFF}	Offset Error	$-40^\circ C \leq T_A \leq 125^\circ C$	± 0.1	± 1.2	LSB (max)
GE	Gain Error	$-40^\circ C \leq T_A \leq 125^\circ C$	± 0.2	± 1.2	LSB (max)



The ADC121S101 is pin compatible with the AD7476 and has better performance and lower power than all versions of the AD7476, and it is guaranteed over a range of sample rates. The ADC121S101 will replace any of the AD7476 versions.

Also available are 10-bit and 8-bit pin- and functionally-compatible alternatives for the AD7477 and the AD7478. These alternatives are also better than the AD7477 and the AD7478.

Descriptive Part Numbering



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We have developed a new part numbering scheme which we hope will make our products easier to specify.

The graphics here show the important aspects of the part number, with the first two numeric digits indicating the resolution of the ADC. The next indicates the number of input channels. The next place indicates the interface. This initial offering concentrates on providing an industry-standard SPI interface compatible with a wide range of industrial microcontroller products.

The inset clarifies the three speed grades we offer relative to the three resolutions. However, the last three digits can sometimes seem arbitrary against this stated standard.

Example: ADC122S101

- 12-bit, 2-channel, SPI interface, 1 MSPS, single supply

8-pin MSOP Pkg 3 x 5 mm

No external components needed

V_A used as reference

SPI Clock is used as ADC clock

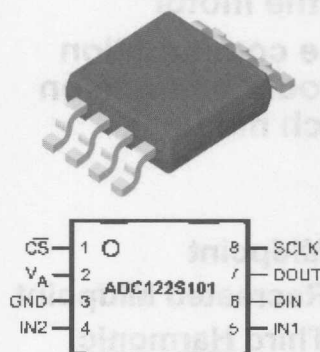
Outstanding performance

ENOB: 11.7 bits (typ)

DNL: +0.9/- 0.6 LSB (typ)

INL: ± 0.64 LSB (typ)

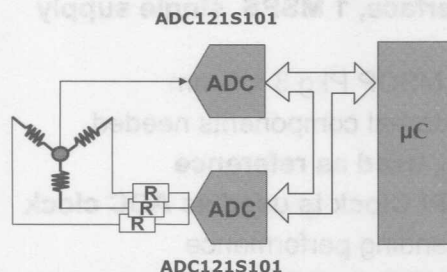
4.3 mW (typ) at 3V Supply



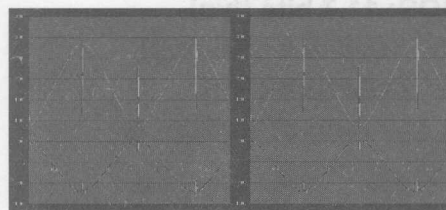
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Here is an example of our newer products. All of our newer 12-bit offerings have about the same performance indicated here, whether 1-, 2-, 4-, or 8-input channels. Similar products of different resolutions are pin and functionally compatible with each other.

Third Harmonic Sensorless Brushless DC Motor Monitor



- ADC1 – ADC2 is the third harmonic of the motor
- The commutation should be done on each min/max



- Midpoint
- Recreated Midpoint
- Third Harmonic

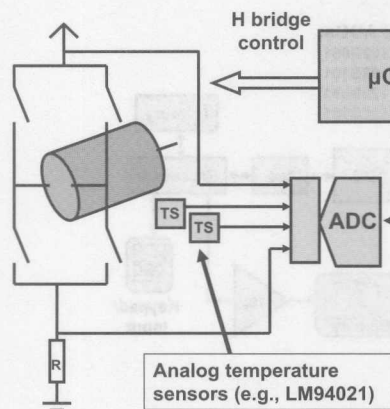
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One way to control a brushless DC motor without Hall sensors is to monitor the third harmonic. This method is detailed in IEEE article, "Indirect sensing for rotor flux position of permanent magnet AC motors operating over a wide speed range". This method is an alternative to the zero crossing back EMF method and has numerous benefits such as wider operating speed range, higher precision, and high acceleration/deceleration rate acceptance. It also can work with PWM control and without mid-point access.

The method is based on the fact that the voltage between the mid-point and the recreated mid-point (with the 3 resistors) is the third harmonic of the motor. Each minimum or maximum of this signal will represent the commutation time for the switcher.

This solution implements two single ADCs in a simultaneous sampling configuration. It also can be implemented with a differential amplifier when the resistors are perfectly matched, but this might be more expensive than the use of a second ADC.

General Purpose ADCs Are Also Used for Peripheral Control



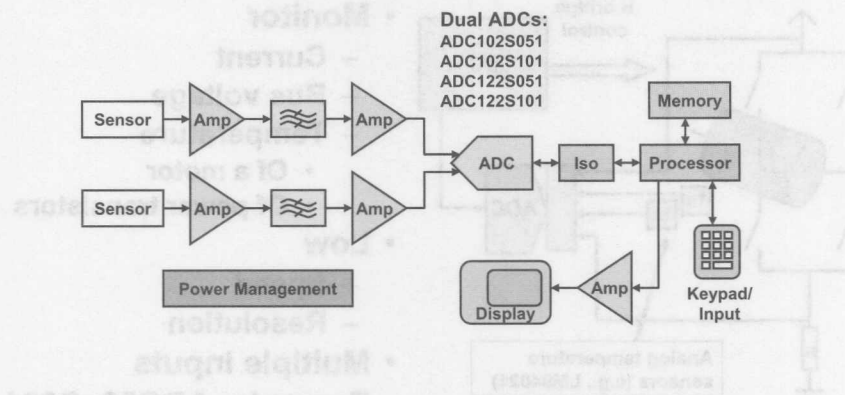
- **Monitor**
 - Current
 - Bus voltage
 - Temperature
 - Of a motor
 - Of power transistors
- **Low**
 - Speed
 - Resolution
- **Multiple inputs**
- **Example: ADC08xS021**

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One common application is the monitoring of a motor's performance: Bus voltage, current drawn, temperature, speed, and vibration. Small ADCs with an input multiplexer can easily fit the small form factor of motor drives.

Medical Patient Monitor



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This patient monitor application has the same precision requirements as does any data acquisition system. The ADC resolution and sample rate will be determined by the sensors chosen, but a serial output ADC will limit the number of data lines required, easing the isolation interface requirements. Using a dual ADC eliminates the multiplexer that would otherwise be needed.

Customer Problem: Read and Understand the Datasheet!

- Problem: Cannot select the channel AIN2 of ADC122S051
- Holding DIN pin low to select AIN1, high to select AIN2
- Solution: DIN must be low during ADD1 time

TABLE 1. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

TABLE 2. Control Register Bit Descriptions

Bit #:	Symbol:	Description
7 - 6, 2 - 0	DONTC	Don't care. The value of these bits do not affect the device.
3	ADD0	These three bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in Table 3.
4	ADD1	
5	ADD2	

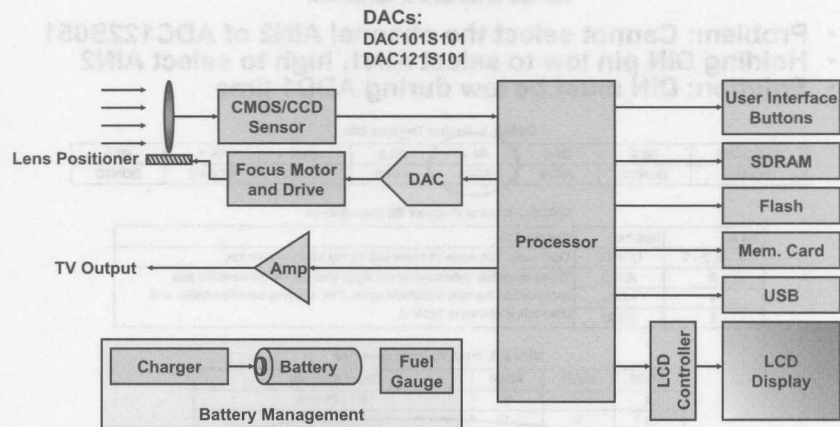
TABLE 3. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
x	0	0	IN1 (Default)
x	0	1	IN2
x	1	x	Not allowed. The output signal at the D_{OUT} pin is indeterminate if ADD1 is high.



The datasheet indicates that the DIN line must be low for the ADD1 (Bit4) time. If this is violated, channel IN2 will not be selected.

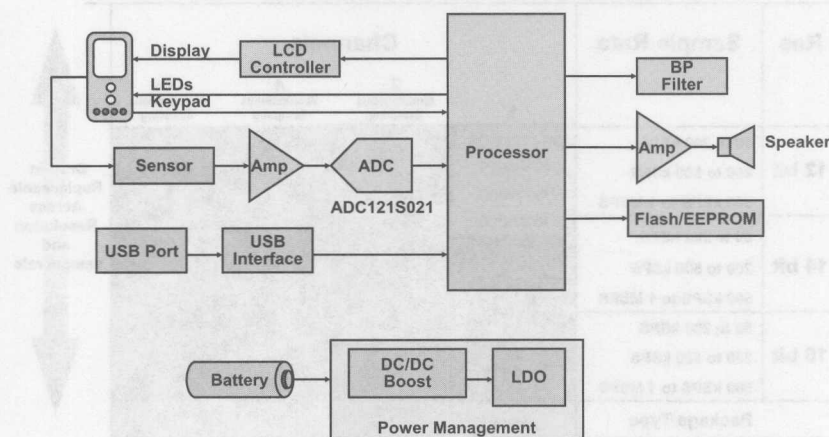
Digital Still Camera Auto Focus



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The DAC is used here to provide a driving voltage to the auto-focus motor. The DACs shown here are well-suited for this application. For faster speeds, the DAC101S051, DAC101S101, DAC121S051, or the DAC121S101 are good candidates.

Blood Glucose Monitor



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The blood glucose monitor is yet another example of a use for a general-purpose ADC. We show the ADC121S021 in this application.

Second New GPADC Family 12-/14-/16-Bit Resolution

SPI/Serial Interface, Differential Input, Ext. Reference

Res	Sample Rate	Channels			
		1	2 Simultaneous Sampling	4 Simultaneous Sampling	8 Simultaneous Sampling
12 bit	50 to 200 kSPS	ADC121S625	In Design		
	200 to 500 kSPS	In Design	In Design		
	500 kSPS to 1 MSPS	In Design	In Design		
14 bit	50 to 200 kSPS				
	200 to 500 kSPS				
	500 kSPS to 1 MSPS		Requires	Definition	
16 bit	50 to 200 kSPS				
	200 to 500 kSPS				
	500 kSPS to 1 MSPS				
Package Type		MSOP-8	MSOP-8, MSOP-10		

Drop-in
Replaceable
Across
Resolution
and
sample rate

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National's second family of new ADCs will cover resolutions from 12 to 16 bits. The ADC121S625 is the first product in this family with a differential input and an external reference.

We have higher-sample-rate 12- and 14-bit, single-channel ADCs, as well as simultaneous sampling ADCs in development. These provide two discrete ADC channels and are targeted at motor-control applications, one of the most common general-purpose ADC applications. In motor control, customers need to have ADC measurements taken at the same time so that the phase relationship is known. These devices will also be well-suited to AC power measurement.

SAR ADC Family Value Proposition

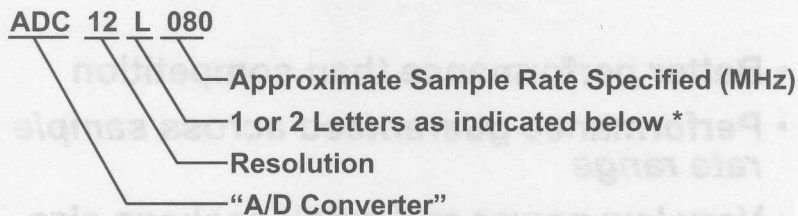
- **Better performance than competition**
- **Performance *guaranteed across sample rate range***
- **Very low power and small package size**
- **Standardized pin out with same input impedance**
- **Easy migration across resolution and sample rate**



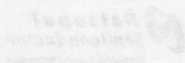
Our processes and design have allowed us to develop a new family of general-purpose ADCs with better performance and lower power consumption than competitive products.

Our performance guarantee over a range of clock rates is unique. Our standardized pin out means one board layout for each channel configuration and that one of National's ADCs may replace several competitive products. All of this simplifies testing and reduces both development cost and inventory for customers who use multiple ADCs.

Part Numbering Convention for High-Speed ADCs

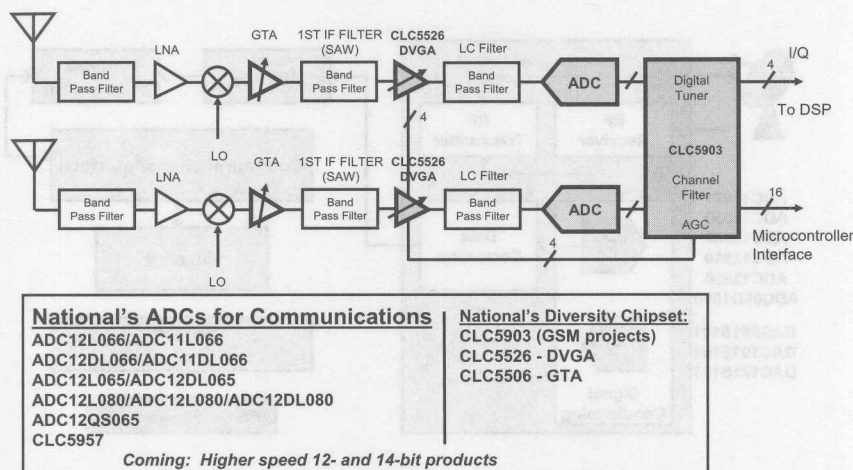


- * D – Dual
- T – Triple
- Q – Quad
- L – Low Voltage (3.3V or less)
- B – FIFO Buffer
- S – Serial (LVDS/SLVS) Outputs



While there are some exceptions to this method of specifying our products, this method generally holds for newer devices. The letters following the resolution may be combined, as in the cases of the ADC12DL066, which is a dual, low-voltage, 12-bit, 66 MSPS ADC.

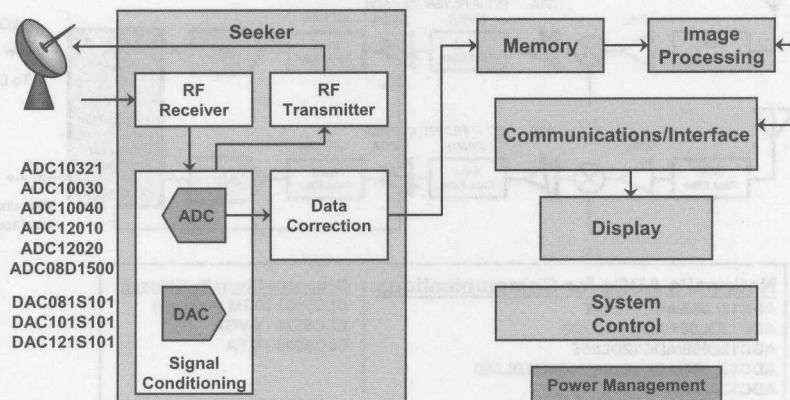
Example Application: Communications Receiver



Our high-speed products provide superior performance in communication systems, as well as in medical and general instrumentation, radar, and other systems requiring high sample rates, including those where undersampling is used. These systems are very demanding and our converters are up to the task.

Shown here is our "diversity receiver chip set," consisting of the CLC6628 Digital Variable Gain Amplifier (DVGA), any of the ADCs listed here, and the CLC5903 digital tuner. In this application, there are two identical channels. The diversity is in either polarization, where one antenna is vertically polarized and the other is horizontally polarized, or in space, where they are separated from each other. When fading occurs, it usually does not happen in both channels at once. The strongest signal is the one that is accepted by the digital tuner.

Radar System



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Radar systems vary quite a lot in their architecture, depending upon the exact application. The A/D converter used can be 10 to 12 bits at relatively low sample rates, or can be 8 bits at a very high sample rate. The ADCs shown here are just some of the choices and include the following:

10-bit, 20 MSPS ADC10321

10-bit, 28 MSPS ADC10030

10-bit, 40 MSPS ADC10040

12-bit, 10 MSPS ADC12010

12-bit, 20 MSPS ADC12020

Dual 8-bit, 1.5 GSPS ADC08D1500, which can operate as a single 8-bit 3 GSPS ADC.

The D/A converter is generally a fairly low sample rate and can be 8 to 12 bits, again depending upon architecture. These are 8-, 10- and 12-bit DACs with conversion rates up to 1.7 MSPS.

ADC12DL066

Dual 12-bit, 66 MSPS ADC

Features

- Wide dynamic range
- IF sampling capability
- Full power bandwidth – 450 MHz
- 2V_{P-P} diff. input range
- On-chip reference buffer
- Pipeline architecture with digital error correction
- 3.3V supply
- 64-pin TQFP package

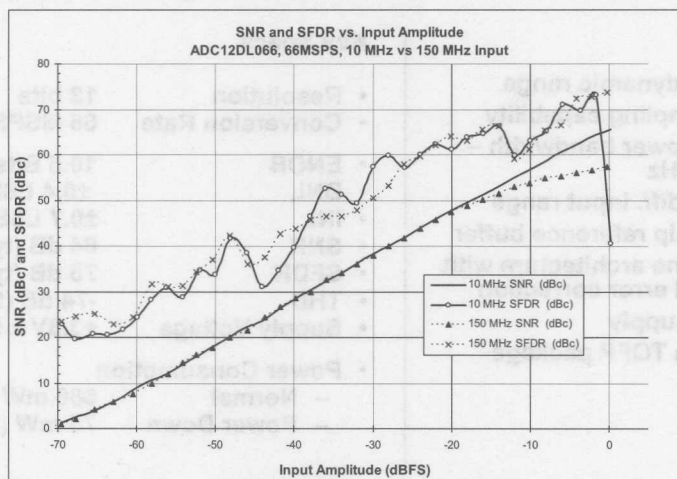
Key Specs

- | | |
|---------------------|-----------------|
| • Resolution | 12 bits |
| • Conversion Rate | 66 MSPS (min) |
| • ENOB | 10.5 Bits (typ) |
| • DNL | ±0.4 LSB (typ) |
| • INL | ±0.7 LSB (typ) |
| • SNR | 64 dB (typ) |
| • SFDR | 78 dB (typ) |
| • THD | -74 dB (typ) |
| • Supply Voltage | +3.3V ± 5% |
| • Power Consumption | |
| – Normal | 686 mW (typ) |
| – Power Down | 75 mW (typ) |



The ADC12DL066 is one of our dual, high-speed, 12-bit ADC offerings. As with those other products, the ADC12DL066 offers excellent performance at low power consumption levels, together with a very high (450 MHz), full power bandwidth.

ADC12DL066: 10 MHz and 150 MHz Input Amplitude SNR and SFDR



The excellent performance of the ADC12DL066 over a wide range of input levels, at both 10 MHz and at 150 MHz input frequencies, can be seen here. Note the near ideal level of performance.

ADC12DL040/ADC12DL065

Dual 12-bit 40/65 MSPS

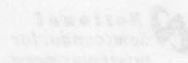


Features

- Industry's Lowest power consumption
- Single +3V/3.3V operation
- On chip precision reference
- Straight binary or 2's complement outputs
- Duty cycle stabilizer
- Parallel or Mux'd outputs
- 64-pin TQFP package
- Pin compatible ADCs:
 - ADC12DL066
 - ADC12D040

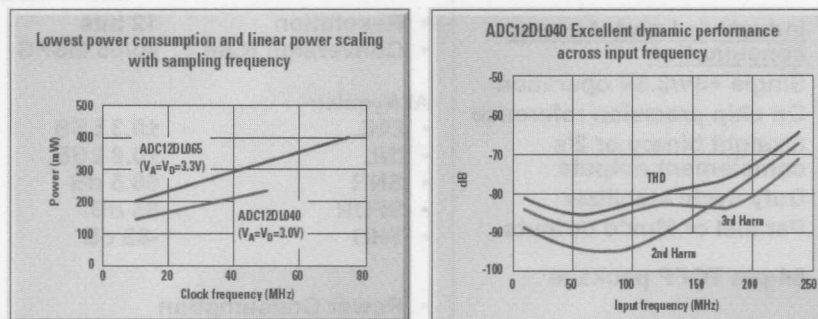
Key Specs

- Resolution 12 bits
- Conversion Rate 40/65 MSPS
- At Nyquist:
 - DNL ± 0.3 LSB
 - INL ± 0.8 LSB
 - SNR 68.5 dB
 - SFDR 85 dB
 - THD -83 dB
- Power Consumption
 - Normal 210/360 mW
 - Power down 36 mW



This recently introduced dual ADC offers excellent performance with extremely low power consumption. The 250 MHz full power bandwidth and dual nature of this device, together with its excellent performance, enables efficient, space-, and cost-saving designs of many systems, including communications and instrumentation, among others. A single, 5V, 40 MSPS version (ADC12040) is available and is pin-compatible with our other 12-bit high-speed ADCs.

ADC12DL040/65 Performance Charts

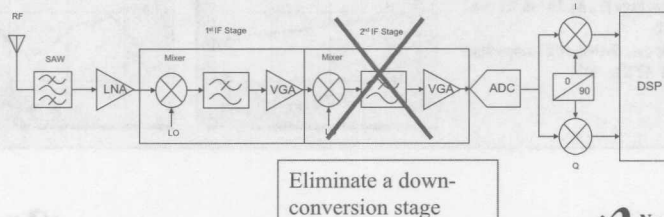
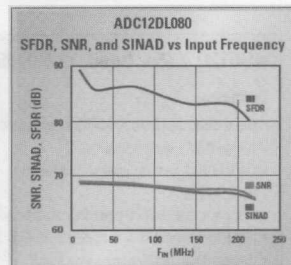


The low power consumption of the ADC12DL040 and of the ADC12DL065 scales in a linear manner with sample rate so that there is no excess power consumption when operating at lower sample rates. Note also the excellent distortion performance, even at very high input frequencies.

ADC12DL080

Industry's Highest IF Sampling Dual 12-bit/80 MSPS ADC

- 600 MHz Bandwidth – best in class
- 200 MHz IF sampling capability
 - Allows flexibility in frequency planning
 - Helps eliminate down conversion stages
 - Reduces system power consumption
 - Improves system reliability



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The ADC12DL080 is a dual, low-power, 12-bit, 80 MSPS ADC intended for IF sampling applications. The 600 MHz bandwidth is the best in the industry with flat dynamic performance up to 200 MHz, another best in the industry. This makes the ADC12DL080 very attractive for high IF sampling applications, providing the following system benefits:

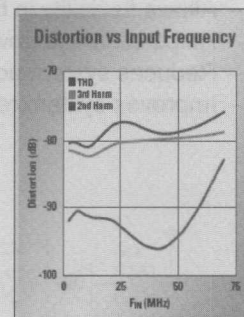
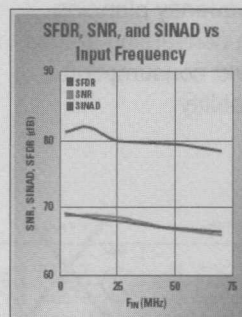
1. Flexibility in frequency planning
2. Eliminate a down conversion stage
3. Reduction in power consumption and improving system reliability

ADC12QS065: Quad, 12-bit, 65 MSPS ADC with Serial LVDS Outputs

ADC12QS065 – Quad, 12-Bit, 65 MSPS ADC with Serial LVDS Outputs

Features

- Quad-channel, 12-bit, 65 MSPS sampling rate
- Single 3.3V supply operation
- Serial LVDS outputs enabling reduced trace count
- Clock and frame LVDS pairs for data capture
- 780 Mbps serial LVDS data rate at 65 MSPS
- Power-down mode consuming 3 mW
- LLP-60 package (9 x 9 x 0.8 mm, 0.5 mm pin pitch)
- Operates over the industrial temperature range of -40°C to +85°C

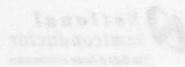


The quad, 12-bit, 65 MSPS ADC12QS065 has serial LVDS outputs and is intended for applications that require multiple high-speed ADCs, such as a medical ultrasound system. The serial LVDS outputs reduce the number of output lines and minimize the noise caused by high capacitances on the digital outputs.

12-/14-bit Family

Product ID	Resolution (bits)	Speed (MSPS)	Power (mW)	ENOB (bit)	SINAD (dB)	SNR (dB)	SFDR (dB)	THD (dB)	Full Power Bandwidth (MHz)	Packaging
ADC12010	12	10	160	11.3	69	70	83	-79	100	LQFP-32
ADC12020	12	20	185	11.3	69	70	86	-83	100	LQFP-32
ADC12040	12	40	340	11.2	69	70	84	-80	100	LQFP-32
ADC12L063	12	62	354	10.3	65	66	78	-74	170	LQFP-32
ADC12L066	12	66	357	10.7	66	66	80	-77	450	LQFP-32
ADC12L080	12	80	425	10.7	66	66	80	-77	450	LQFP-32
ADC12D040	12-bit dual	40	600	10.9	68	68	80	-78	100	TQFP-64
ADC12DL040	12-bit dual	40	210	11.1	69	69	86	-83	250	TQFP-64
ADC12DL065	12-bit dual	65	360	11.1	69	69	86	-84	250	TQFP-64
ADC12DL066	12-bit dual	66	686	10.7	66	66	81	-78	450	TQFP-64
ADC12DL080	12-bit dual	80	447	11	69	69.3	82	-80	600	TQFP-64
ADC12QS065	12-bit quad	65	800	11.1	68.3	68.5	85	-83	300	LLP-60
ADC14L020	14	20	150	12	74	74	93	-90	150	LQFP-32
ADC14L040	14	40	235	11.9	73	73.3	90	-86	150	LQFP-32

- Low-power, pin-compatible family
 - ADC12010/20/40
 - ADC12L063/66/80
 - ADC12DL040/65/80
 - ADC14L020/40b
- High full power bandwidth
- Power-down feature
- Parallel CMOS and Serial LVDS outputs



National's 12- and 14-bit high-speed ADCs include singles, duals, and a quad with sample rates up to 80 MSPS and impressive performance for the power consumed.

10-bit Family

	Speed (MSPS)	Power (mW)	ENOB (bit)	SINAD (dB)	SNR (dB)	SFDR (dB)	THD (dB)	Full Power Bandwidth (MHz)	
Product ID									Packaging
ADC10321	20	98	9.5	59	60	72	-70	150	LQFP-32
ADC10030	27	125	9.4	58	60	68	-66	150	LQFP-32
ADC10040	40	55.5	9.6	59	59	80	-77	400	TSSOP-28
ADC10065	65	68.4	9.5	59	59	80	-72	400	TSSOP-28
ADC10080	80	78.6	9.5	59	59	79	-75	400	TSSOP-28
ADC10D020	20	150	9.5	59	59	75	-73	140	TQFP-48
ADC10D040	40	257	9.5	59	60	72	-69	140	TOFP-48

- Low power pin compatible family
 - ADC10040/65/80
 - ADC10D020/40
- Power scales with clock speed (ADC10040/65/80)
- Multiplexed or parallel outputs on the duals
- Power down feature
- Selectable gain with the ADC10040/65/80



Our 10-bit, high-speed offering currently includes wide input bandwidths with speeds of 20 MSPS to 80 MSPS and quite impressive Effective Number of Bits (ENOBs).

Low-Power, 8-/10-bit Family

Product ID	Resolution (bits)	Speed (MSPS)	Pin/Function Compatible	Power (mW)	ENOB (bit)	SNR (dB)	SFDR (dB)	Full Power Bandwidth (MHz)	Packaging
ADC1173	8	15	↑ ↓	33	7.6	49	55	120	SOIC-24, TSSOP-24
ADC1175	8	20		60	7.3	47	58	120	SOIC-24, TSSOP-24
ADC1175-50	8	50		125	7.2	45	56	120	LLP-24, SOIC-24, TSSOP-24
ADC08351	8	42	↑ ↓	40	6.8	44	49	120	TSSOP-20
ADC08060	8	60		78	7.6	47	63	200	TSSOP-24
ADC08L060	8	60		39	7.6	48	59	270	TSSOP-24
ADC08100	8	100		130	7.5	47	60	200	TSSOP-24
ADC08200	8	200	↑ ↓	210	7.3	46	60	500	TSSOP-24
ADCS9888	8-bit triple	140, 170, 205		1290	—	44	—	500	PQFP-128
ADC10321	10	20		98	9.5	60	72	150	LQFP-32
ADC10030	10	27		125	9.4	60	68	150	LQFP-32
ADC10040	10	40	↑ ↓	55.5	9.6	59	80	400	TSSOP-28
ADC10065	10	65		68.4	9.5	59	80	400	TSSOP-28
ADC10080	10	80		78.6	9.5	59	79	400	TSSOP-28
ADC10D020	Dual 10-bit	20		150	9.5	59	75	140	TQFP-48
ADC10D040	Dual 10-bit	40	↑ ↓	257	9.5	60	72	140	TQFP-48

- Power scales with clock speed
- Multiplexed or parallel outputs on 10-bit dual ADCs
- Power down feature
- Selectable input swings



Our 8-bit, high-speed ADC offering includes specified sample rates from 15 MSPS to 205 MSPS. Products above these sample rates are our ultra-high-speed products, while our 10-bit high speed offering currently includes high input bandwidths with speeds of 20 MSPS to 80 MSPS and quite impressive ENOB.

Low-Power 12-/14-bit Family

Product ID	Resolution (bits)	Speed (MSPS)	Pin/Function Compatible	Power (mW)	ENOB (bit)	SNR (dB)	SFDR (dB)	Full Power Bandwidth (MHz)	Packaging
ADC12010	12	10	↑	160	11.3	70	83	100	LQFP-32
ADC12020	12	20		185	11.3	70	86	100	LQFP-32
ADC12040	12	40		340	11.2	70	84	100	LQFP-32
ADC12L063	12	62		354	10.3	66	78	170	LQFP-32
ADC12L066	12	66	↓	357	10.7	66	80	450	LQFP-32
ADC12L080	12	80		425	10.7	66	80	450	LQFP-32
ADC12D040	12-bit dual	40		600	10.9	68	80	100	TQFP-64
ADC12DL040	12-bit dual	40		210	11.1	69	86	250	TQFP-64
ADC12DL065	12-bit dual	65	↓	360	11.1	69	86	250	TQFP-64
ADC12DL066	12-bit dual	66		686	10.7	66	81	450	TQFP-64
ADC12DL080	12-bit dual	80		447	11	69.3	82	600	TQFP-64
ADC12QS065	12-bit quad	65		800	11.1	68.5	85	300	LLP-60
ADC14L020	14	20	↑	150	12	74	93	150	LQFP-32
ADC14L040	14	40		235	11.9	73.3	90	150	LQFP-32

- High full power bandwidth
- Power scales with clock speed
- Parallel CMOS and LVDS outputs
- Power-down feature



National's 12- and 14-bit high-speed ADCs include pin-compatible families of singles, duals, and a quad with sample rates up to 80 MSPS and impressive performance for the power consumed. Some of these products, like the ADC12L066, ADC12DL066, and ADC12DL080, feature high input bandwidths, and our data output formats offered are parallel CMOS and serial LVDS (ADC12QS065).

ADC08D1000

Dual, 8-bit 1 GSPS ADC

Features

- Single 1.9V power supply
- Output data rate
 - 1:2 demux: 2 output channels interleaved to provide 500 MSPS/channel (LVDS)
- Differential inputs
- Internal voltage reference
- Buffered internal sample and hold
- Dual edge sampling (interleaving)
- Double Data Rate support
- Synchronization between multiple channels
- Full-scale (gain) and offset adjustment of each ADC (I & Q).
- 128-pin EP LQFP package

Key Performance Metrics

- Resolution 8 bits
- Conversion rate: 1 GSPS

Specifications at $F_{IN} = 500$ MHz

- ENOB 7.4 bits
- DNL ± 0.15 LSB
- INL ± 0.30 LSB
- SNR 47.1 dB
- SFDR 55 dB
- SINAD 46.3 dB
- THD -55 dB
- Power consumption
 - Normal Operation: 1.6W (typ)
 - Power Down Mode: 20 mW



The ADC08D1000 is a dual, 1 GSPS ADC with input channels labeled I and Q.

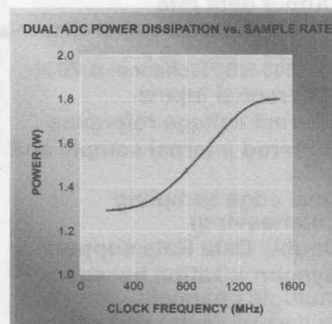
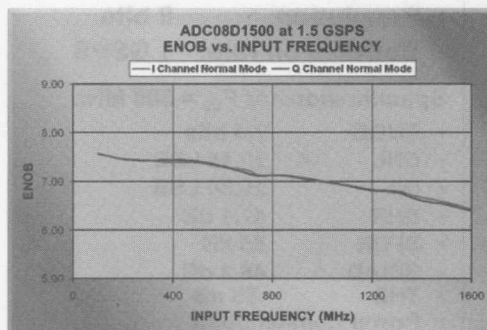
Both converters on the die have fully differential inputs with a maximum input signal range of 950 mV_{p-p}. Each converter has a 1:2 demultiplexer that feeds two LVDS buses and reduces the output data rate on each bus to half the sampling rate. A choice of SDR and DDR is available and an output data clock eases data capture.

The two converters may be interleaved such that they both sample the input signal at the user's choice of either input. In this Dual Edge Sampling (DES) mode, the two converters sample the one signal on opposite edges of the ADC input clock, so that the net sample rate is twice the input clock frequency. Since the ADC08D1000 is specified for 1 GSPS, the overall sample rate in the DES mode is guaranteed at 2 GSPS. Since the ADC08D1000 will typically perform at 1.3 GSPS, the DES mode can provide a 2.6 GSPS conversion rate.

ADC08D1000

Unparalleled Performance!

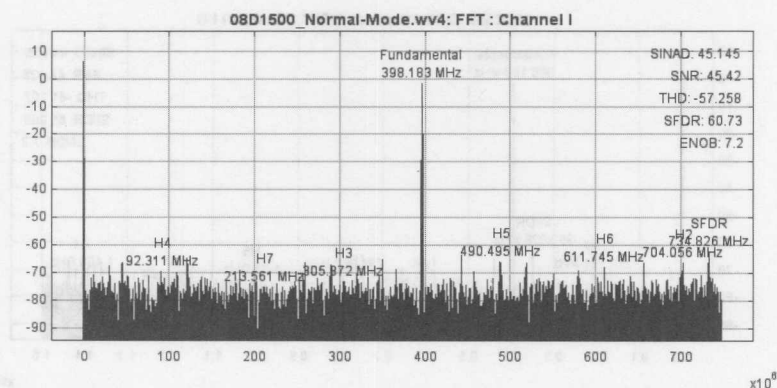
Low-Power



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The ADC08D1000 maintains excellent performance over its full input frequency range and consumes very little power in doing so. This performance is achieved by incorporating trimmed input termination resistors at the analog signal inputs, avoiding the stub problems commonly seen when input termination is done on the printed circuit board.

ADC08D1500 Frequency Domain Plot (Normal Mode)

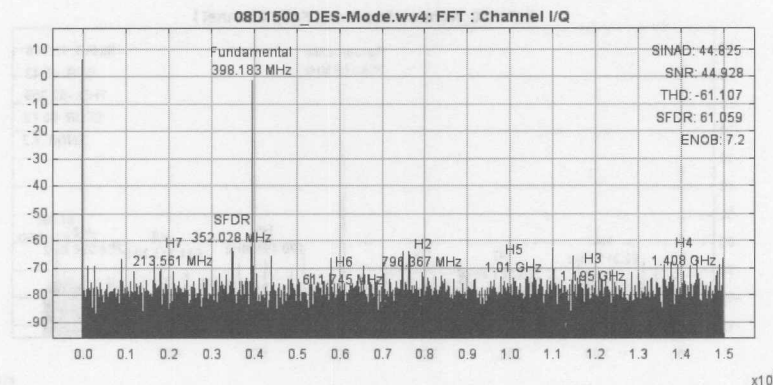


Best performance is obtained in the normal mode. Note the excellent performance obtained at this very high sample rate (1.5 GSPS).

This data was taken with our ADC08D1500 development system, which should represent what can be realized in an actual circuit. Our evaluation board produces somewhat better performance than shown here.

Competitive solutions require 10 bits, with the attendant large power consumption, to get an ENOB of just 7.0!

ADC08D1500 Frequency Domain Plot (Dual Edge Sampling Mode)

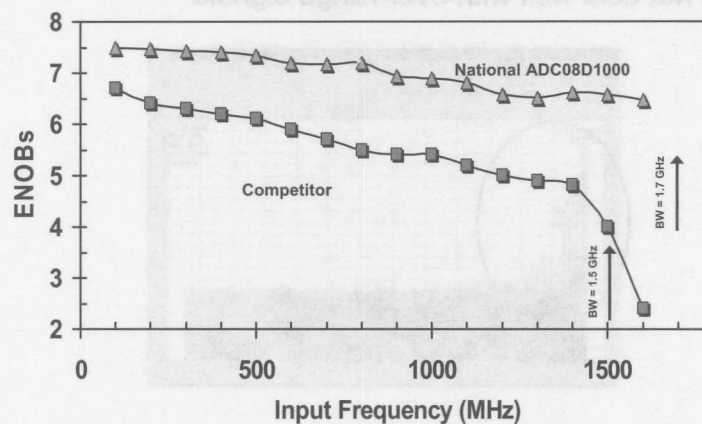


The performance in the DES mode is very close to what can be achieved in the normal mode. This excellent performance obtained at a 3.0 GSPS rate with our ADC08D1500 development system, which should represent what can be realized in an actual circuit. As is true in the normal mode, our evaluation board produces somewhat better performance than shown here.

Nowhere else will you get this high a performance at this sample rate.

Competitive Stance

1 GSPS, SPI Mode with default settings

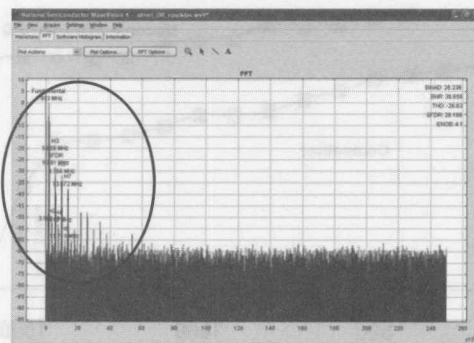


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This input sweep demonstrates how our ADC08D1000 performs against our only competition. Note that the National ADC08D1000 is consistently about 1 ENOB better. Also, as the frequency gets higher, the difference between the two devices widens.

Comments on Competitive Product

- Many spurs as the input gets close to 1.5 GHz
- Does not deal well with over-range signals



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The bandwidth of the competition becomes an issue at 1.5 GHz, but, more importantly, many spurs show up as the input gets close to 1.5 GHz.

Another problem with the competitive offering is that it does not deal well with over-range signals. This is important for test equipment applications.

Signal Translations LVDS, LVPECL, and CML

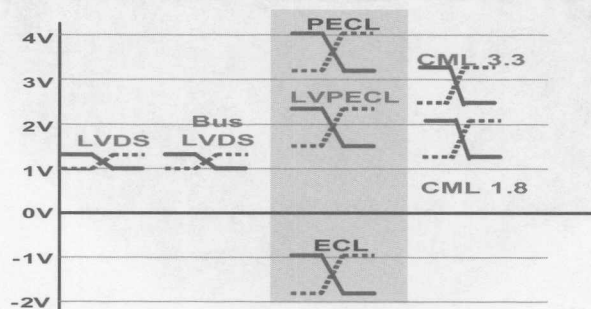
Today, three commonly used interfaces, Low Voltage Differential Signal (LVDS), Low Voltage Positive Emitter-Coupled Logic (LVPECL), and Current Mode Logic (CML) are commonly used for data transmission. When designing these systems, we often encounter the problem of how to connect different ICs with different signaling levels.

To maximize performance, a good understanding of input and output circuit configurations, biasing, coding, and termination is required.

This presentation provides various methods to properly interface LVDS, LVPECL, and CML devices.

Differential I/O Comparisons

	LVDS (3.3V)	LVPECL (3.3V)	CML (3.3V)
Offset	1.2V	2V	3.1V
Output Swing (Single Ended)	250 to 450 mV	600 to 900 mV	300 to 500 mV
Input Swing (Single Ended)	50 to 1000 mV	310 to 1000 mV	200 to 600 mV
Output Differential (VOD)	500 to 900 mV	1200 to 1800 mV	600 to 1000 mV
Input Differential (VID)	100 to 2000 mV	620 to 2000 mV	400 to 1200 mV



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The figure and table show some typical interface levels for differential transmission technologies. LVDS, LVPECL, and CML feature different swings and different offset voltages.

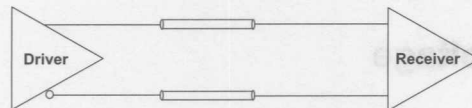
LVDS is standardized (ANSI/TIA/EIA-644-A-2001) while LVPECL and CML are not.

To maintain interoperability between devices with different supply and interface levels requires using either direct current (DC) coupling or alternating current (AC) coupling to be employed. We will discuss and show the benefits and drawbacks to using either DC or AC coupling in the following slides.

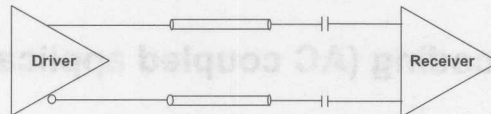
Unless stated otherwise, all references to signal levels are for single-ended measurements.

Level Translation Interfaces

- DC coupling



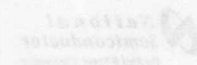
- AC coupling



At the most basic level, there are two methods to interface different logic devices: DC coupling and AC coupling.

Level Translation Considerations

- **Common-mode range**
- **Offset voltage**
- **Termination**
- **Capacitor selection (AC coupled applications)**
- **Data encoding (AC coupled applications)**

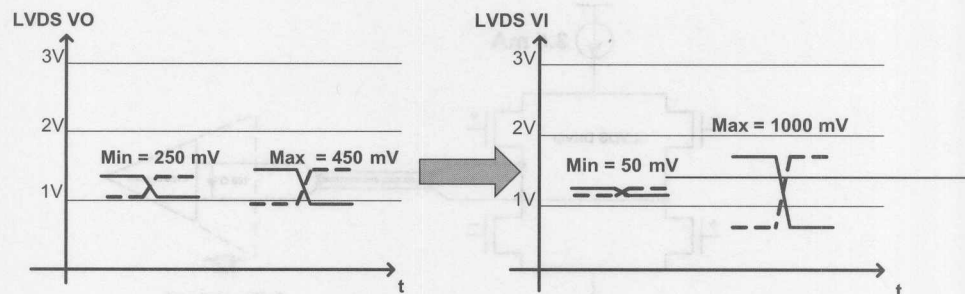


When DC and AC couplings are used to interface LVDS, LVPECL, and CML, the various offset voltages, common-mode ranges, and required terminations should be considered. In addition, for AC coupled applications, data encoding should also be addressed.

Some of National's LVDS devices will directly accept different logic signals such as LVPECL. For more information, please consult device datasheets.

LVDS Interfaces

DC Coupled (1 of 2)



Note: VO = Voltage output/VI = Voltage input

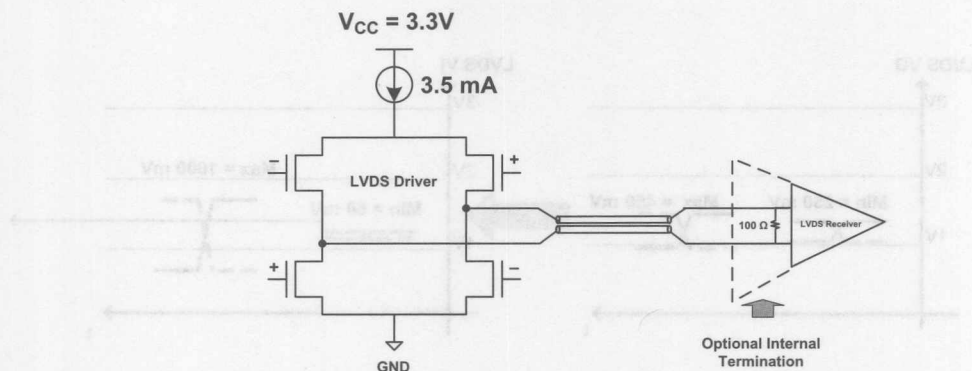


The next few slides show LVDS drivers and receivers with DC Coupling.

This slide shows typical offset voltages between an LVDS driver and receiver.

LVDS I/O Structures

DC Coupled (2 of 2)

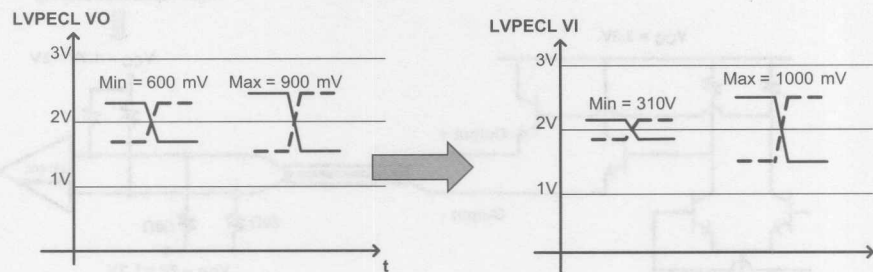


Because LVDS drivers and receivers have the same offset voltages, common-mode range compatibility, and target 100Ω termination resistance, LVDS devices can be DC coupled. They can also be AC coupled. However, for best performance results, some type of data coding or DC balancing should be implemented. DC balancing in AC coupled applications will be discussed in this presentation.

Termination resistors can be external or internal. Currently, National's Bus LVDS and Channel Link products do not offer internal terminations. However, some of National's products do contain internal terminations. For product specific information, please refer to the datasheet or contact your local sales office.

LVPECL Interfaces

DC Coupled (1 of 2)



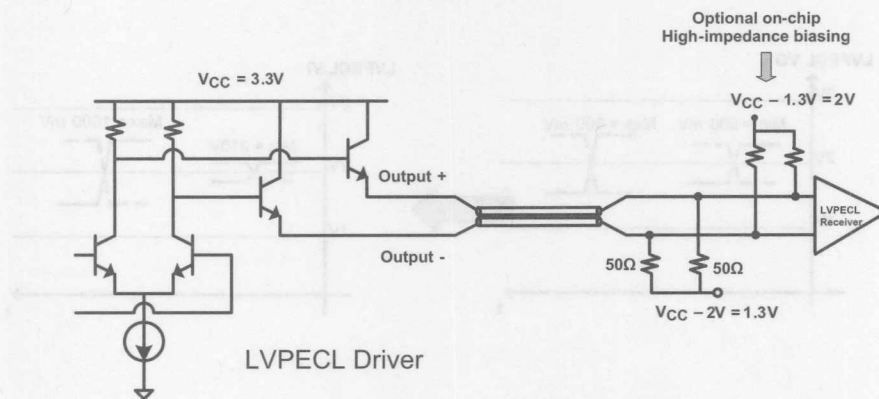
Note: VO = Voltage output/VI = Voltage input



Interfacing LVPECL-to-LVPECL logic devices uses the same DC coupling methodology as LVDS.

LVPECL I/O Structures

DC Coupled (2 of 2)



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As shown above, LVPECL output and input structures are different from LVDS.

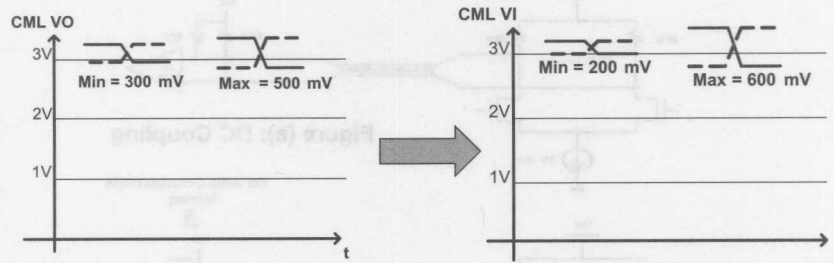
LVPECL uses two 50Ω termination resistors pulled to $V_{CC}-2V$. As such, the differential outputs (Output \pm) will be at $V_{CC}-1.3V$ (2V when using a 3.3V power supply), which results in a DC current flow of 14 mA.

LVPECL devices typically have on-chip high impedance (approximately $1\text{ k}\Omega$) biasing centered at $V_{CC}-1.3V$.

Since LVPECL devices have open emitter outputs, the output emitter followers should operate in the active region with DC current flowing at all times. This increases switching speeds and maintains fast turn-off times.

CML Interfaces

DCIAC Coupled (1 of 2)



Note: VO = Voltage output/VI = Voltage input



This slide shows the typical offset voltages for CML drivers and receivers.

CML I/O Structures

DC/AC Coupled (2 of 2)

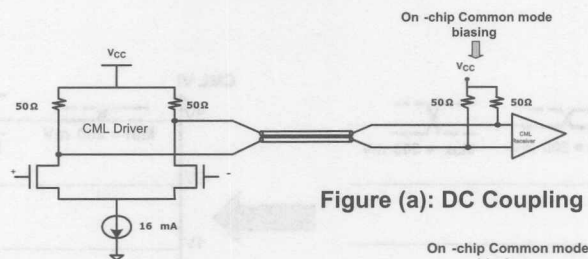


Figure (a): DC Coupling

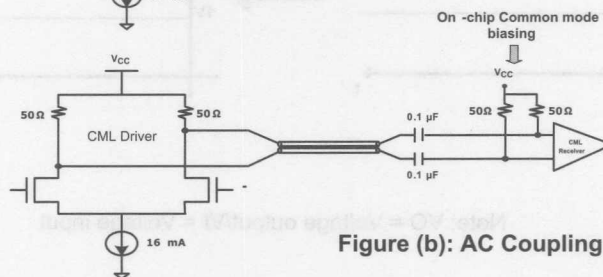


Figure (b): AC Coupling

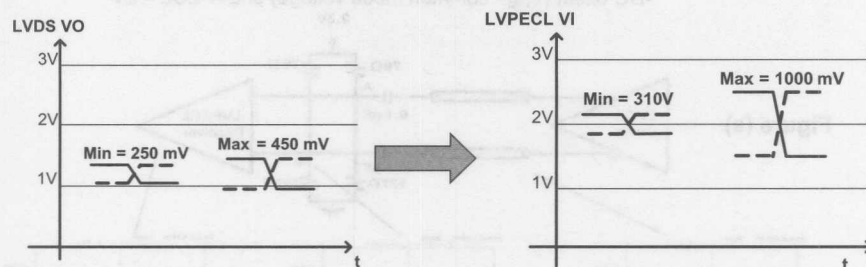
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Figure (a) shows DC coupling for CML interfaces. DC coupling can be used when both the CML driver and receiver meet the following conditions: 1) same power supply voltage; 2) the termination resistors of the receiver connect to V_{CC} internally.

Because CML is not standardized, some receiver input termination resistors may not be tied to V_{CC} or to other voltages. Thus, we recommend using AC coupling (Figure b) between all CML to CML interfaces.

LVDS-to-LVPECL Interfaces

DC/AC Coupled (1 of 5)



Note: VO = Voltage output/VI = Voltage input



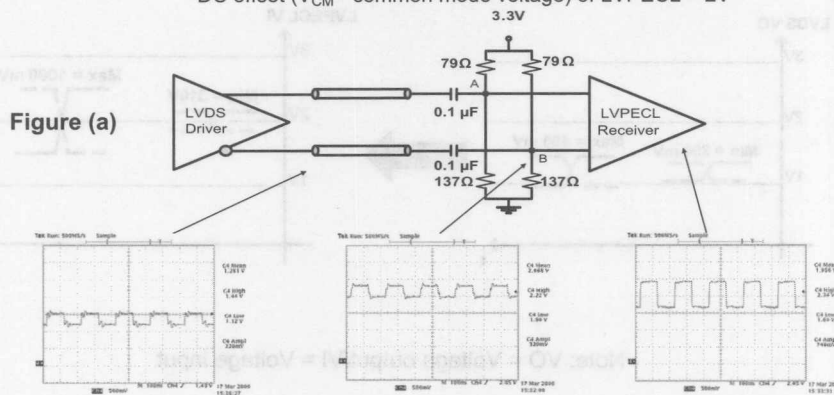
This slide shows the typical offset voltage for an LVDS-to-LVPECL interface. To optimize performance and because the offset voltage requirements differ, level translations should be implemented.

LVDS-to-LVPECL Interfaces

AC Coupled (2 of 5)

LVPECL without on-chip biasing:

- $R_{IN} = 50\Omega$
- DC offset (V_{CM} - common mode voltage) of LVPECL = 2V



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The next two slides describe AC coupling between LVDS and LVPECL.

Figures (a), (b), and (c) show possible termination schemes for an LVPECL receiver that does not have on-chip biasing.

The resistor network resets the offset voltage to 2V and provides an impedance of 50Ω for the LVPECL input.

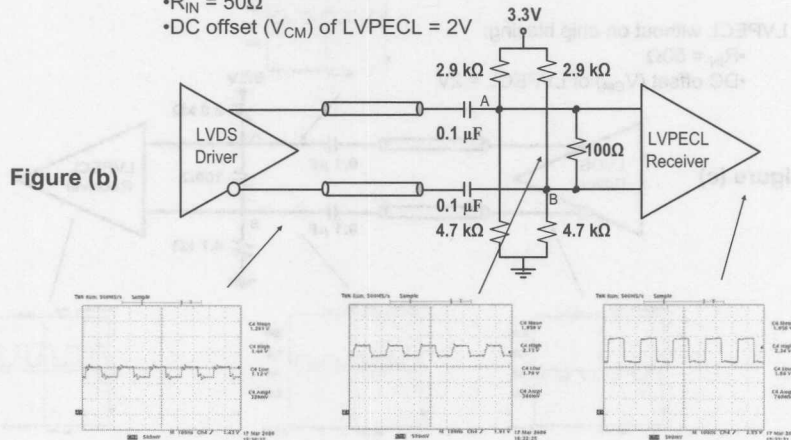
Figure (a) uses low value resistors to provide a single-ended input impedance of 50Ω. The next slide, Figure (b), uses higher-value resistors to reduce power consumption.

LVDS-to-LVPECL Interfaces

AC Coupled (3 of 5)

LVPECL without on-chip biasing:

- $R_{IN} = 50\Omega$
- DC offset (V_{CM}) of LVPECL = 2V



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The next two slides describe AC coupling between LVDS and LVPECL.

Figures (a), (b), and (c) show possible termination schemes for an LVPECL receiver that does not have on-chip biasing.

The resistor network resets the offset voltage to 2V and provides an impedance of 50Ω for the LVPECL input.

Figure (a) uses low-value resistors to provide a single-ended input impedance of 50Ω. The next slide, Figure (b), uses higher-value resistors to reduce power consumption.

LVDS-to-LVPECL Interfaces

AC Coupled (4 of 5)

LVPECL without on-chip biasing:

- $R_{IN} = 50\Omega$
- DC offset (V_{CM}) of LVPECL = 2V

Figure (c)

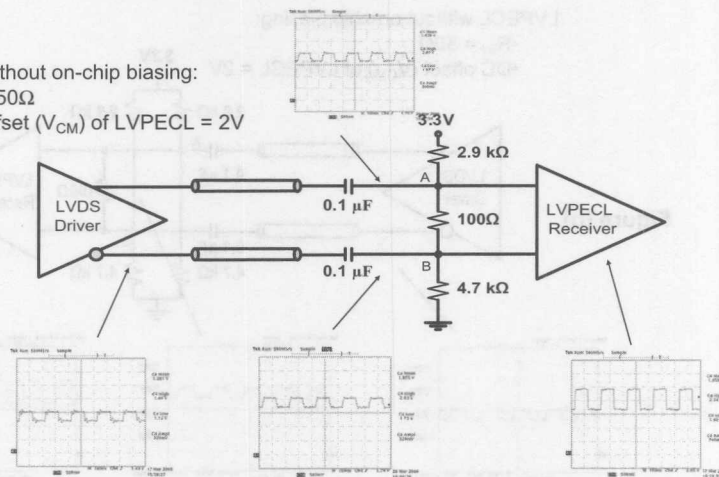


Figure (c) is the simplest way to reduce the total number of components and also has the lowest power consumption. Although there is a slight offset from the nominal LVPECL common-mode voltage, this configuration has the added benefit of failsafe protection. For more information on failsafe biasing, please see the LVDS Owner's Manual.

LVDS-to-LVPECL Interfaces

AC Coupled (5 of 5)

Biasing resistor network comparison:

	Total Component	Offset A	Offset B	Resistor Network I_{CC}	VO @ A or B	Advantage
Fig. (a)	4	2.044V	2.041V	30.85 mA	320 mV	<ul style="list-style-type: none"> • Possible speed advantage
Fig. (b)	5	1.994V	1.995V	1.82 mA	340 mV	<ul style="list-style-type: none"> • Lower power consumption
Fig. (c)	3	1.988V	1.947V	1.58 mA	320mV	<ul style="list-style-type: none"> • Fail Safe feature • Minimum external resistors • Lowest power consumption



This provides a summary of the three different termination-resistor networks.

Figure (c) is the simplest way to reduce the total number of components and also has the lowest power consumption. Although there is a slight offset from the nominal LVPECL common-mode voltage, this configuration has the added benefit of failsafe protection. For more information on failsafe biasing, please see the LVDS Owner's Manual.

LVDS-to-LVPECL Interfaces

AC Coupled (1 of 3)

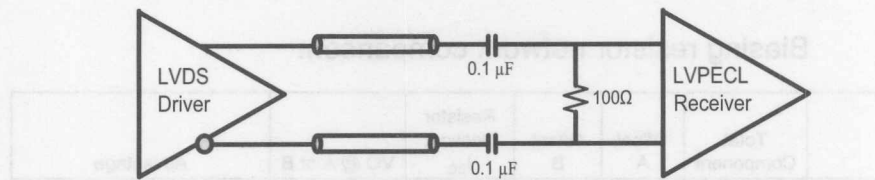


Figure (d): with on-chip biasing

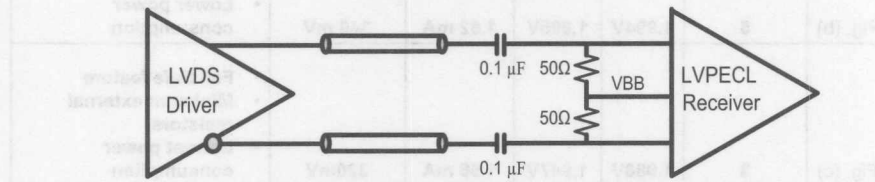


Figure (e): with on-chip internal biasing (VBB)



This slide shows an AC-coupled LVDS to LVPECL interface.

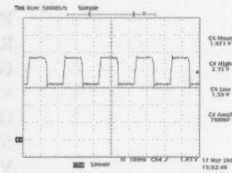
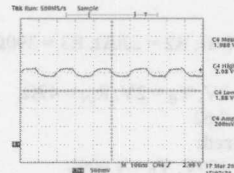
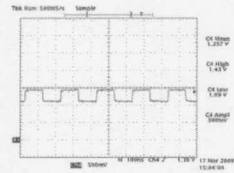
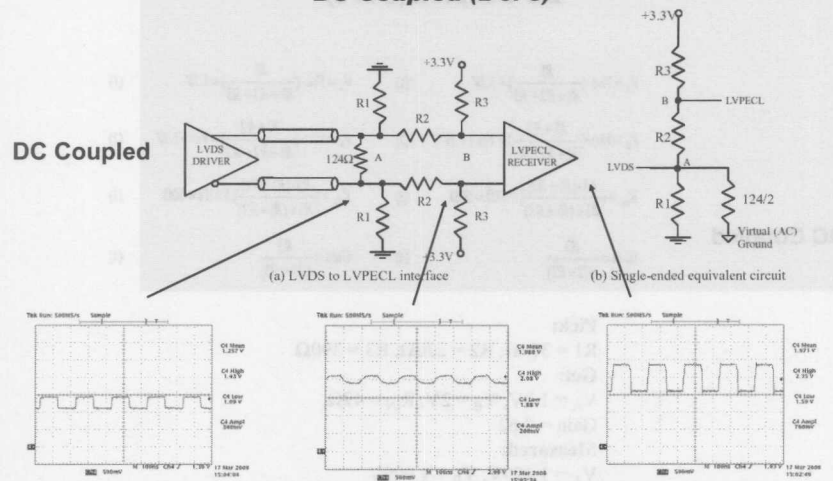
Previously, we stated that some LVPECL devices could have internal biasing at the receiver inputs.

Figure (d) shows an AC-coupled case when an LVPECL receiver input has on-chip biasing.

Alternatively, Figure (e) shows an AC-coupled case when an LVPECL receiver input provides a reference voltage (VBB) at 2V. For this case, two 50 Ω series termination resistors are used.

LVDS-to-LVPECL Interfaces

DC Coupled (2 of 3)



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When DC-coupling LVDS and LVPECL interfaces, use the resistor network shown here. The resistor network shifts the DC from the LVDS offset output ($V_A = 1.2V$) to the LVPECL input ($V_B = 2V$).

Diagram (b) is the single-ended version of diagram (a). Again, for the best performance, the following needs to be considered: 1) offset, 2) termination, and 3) common-mode range.

Because the LVDS output voltage is referenced to ground and the LVPECL input voltage is referenced to V_{CC} , the resistor network shown is used to make the LVDS output less sensitive to power supply variations.

The selection of bias resistor values often involves a trade off between power consumption and speed.

For instance, assuming the LVPECL input parasitic capacitance is small, choosing lower resistor values for R1, R2, and R3 will allow for higher-speed operation. However, with this type of configuration, the total power consumption will increase due to higher current flow through the low-value resistors.

When designing resistor networks, impedance matching ($R_{IN} = 50\Omega$) and network attenuation (Gain > 0.6 with a minimum VOD of LVDS = 500 mV, and min VID of LVPECL = 300 mV) should be considered.

LVDS to LVPECL Interfaces

DC Coupled (3 of 3)

$$V_A = V_{CC} \cdot \left(\frac{R1}{R1 + R2 + R3} \right) = 1.2V \quad (1) \quad V_B = V_{CC} \cdot \left(\frac{R1}{R1 + R2 + R3} \right) = 1.2V \quad (1)$$

$$V_B = V_{CC} \cdot \left(\frac{R1 + R2}{R1 + R2 + R3} \right) = V_{CC} - 1.3V \quad (2) \quad V_B = V_{CC} \cdot \left(\frac{R1 + R2}{R1 + R2 + R3} \right) = V_{CC} - 1.3V \quad (2)$$

$$R_{IN} = \left(\frac{R3 \cdot (R1 + R2)}{R3 + (R1 + R2)} \right) // 62\Omega = 50\Omega \quad (3) \quad R_{IN} = \left(\frac{R3 \cdot (R1 + R2)}{R3 + (R1 + R2)} \right) // 62\Omega = 50\Omega \quad (3)$$

DC Coupled

$$Gain = \frac{R3}{(R2 + R3)} \quad (4) \quad Gain = \frac{R3}{(R2 + R3)} \quad (4)$$

Pick:

R1 = 374Ω, R2 = 220Ω, R3 = 390Ω

Get:

V_A = 1.2V, V_B = 2V, R_{IN} = 49Ω,

Gain = 0.62

Measured:

V_A = 1.199V, V_B = 1.909V

V_O at A = 340 mV, V_O at B = 200 mV

I_{CC} of Network = 7 mA



When DC coupling LVDS and LVPECL interfaces, use the resistor network shown here. The resistor network shifts the DC from the LVDS offset output (V_A = 1.2V) to the LVPECL input (V_B = 2V).

Diagram (b) is the single-ended version of diagram (a). Again, for the best performance, the following needs to be considered: 1) offset, 2) termination, 3) common-mode range.

Because the LVDS output voltage is referenced to ground and the LVPECL input voltage is referenced to V_{CC}, the resistor network shown is used to make the LVDS output less sensitive to power supply variations.

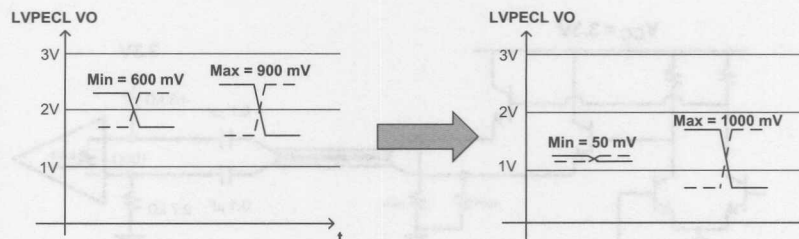
The selection of bias resistor values often involves a trade off between power consumption and speed.

For instance, assuming the LVPECL input parasitic capacitance is small, choosing lower resistor values for R1, R2, and R3 will allow for higher-speed operation. However, with this type of configuration, the total power consumption will increase due to higher current flow through the low value resistors.

When designing resistor networks, impedance matching (R_{IN} = 50Ω) and network attenuation (gain > 0.6 with a minimum VOD of LVDS = 500 mV, and min VID of LVPECL = 300 mV) should be considered.

LVPECL to LVDS Interfaces

DC/AC Coupled (1 of 4)



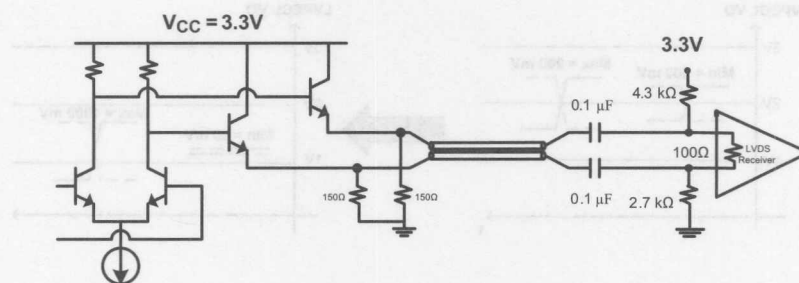
Note: VO = Voltage output/VI = Voltage input



For LVPECL to LVDS interfaces, either AC or DC coupling can be used.

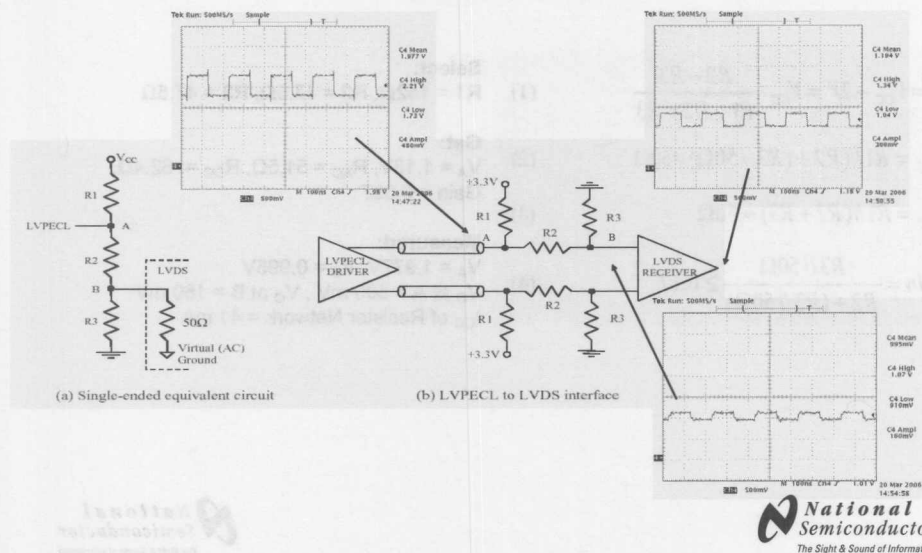
LVPECL-to-LVDS Interfaces

AC Coupled (2 of 4)



This slide shows an AC-coupled application.

LVPECL-to-LVDS Interfaces DC Coupled (3 of 4)



This slide shows a DC-coupled LVPECL-to-LVDS interface. This figure assumes the LVDS device has an internal termination resistor.

LVPECL outputs are optimized for 50Ω loads biased to $V_{CC}-2V$. The resistor network shown primarily serves as a level shifter and attenuator network which addresses this issue.

LVPECL-to-LVDS Interfaces

DC Coupled (4 of 4)

$$V_A = V_{CC} - 2V = V_{CC} \cdot \frac{R2 + R3}{R1 + R2 + R3}$$

$$R_{AC} = R1 // (R2 + (R3 // 50\Omega)) = 50\Omega$$

$$R_{DC} = R1 // (R2 + R3) \approx 50\Omega$$

$$Gain = \frac{R3 // 50\Omega}{R2 + (R3 // 50\Omega)} \geq 0.17$$

Select:

(1) $R1 = 182\Omega, R2 = 47.5\Omega, R3 = 47.5\Omega$

Get:

(2) $V_A = 1.13V, R_{AC} = 51.5\Omega, R_{DC} = 62.4\Omega,$
Gain = 0.337

(3)

Measured:

(4) $V_A = 1.977V, V_B = 0.995V$
 V_O at A = 500 mV, V_O at B = 160 mV
 I_{CC} of Resistor Network = 41 mA

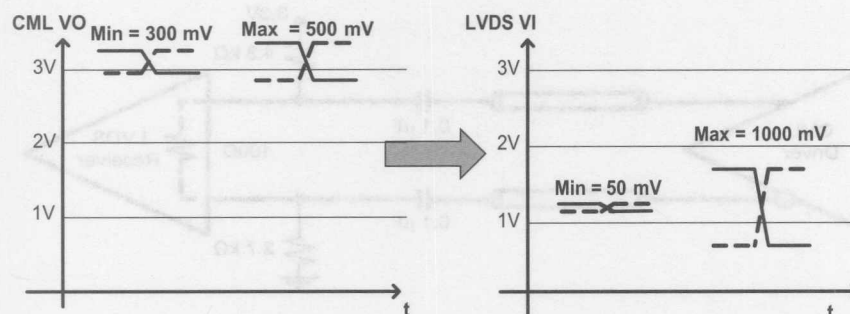


This slide shows a DC-coupled LVPECL-to-LVDS interface. This figure assumes the LVDS device has an internal termination resistor.

LVPECL outputs are optimized for 50Ω loads biased to $V_{CC}-2V$. The resistor network shown primarily serves as a level shifter and attenuator network which addresses this issue.

CML-to-LVDS Interfaces

AC Coupled (1 of 2)



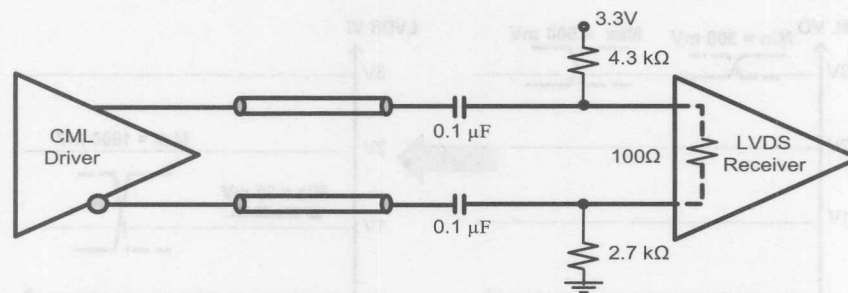
Note: VO = Voltage output/VI = Voltage input



For any CML involved interface, AC coupling is recommended.

CML-to-LVDS Interfaces

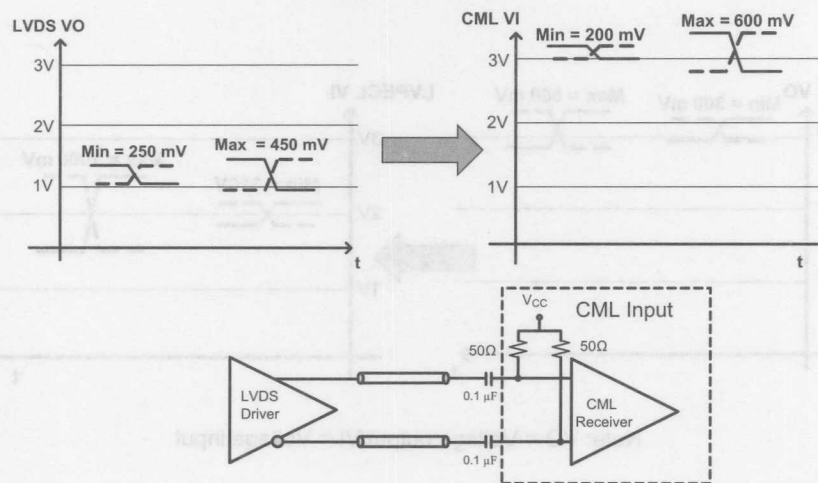
AC Coupled (2 of 2)



The slide presented shows an AC-coupled CML-to-LVDS interface.

LVDS-to-CML Interfaces

AC Coupled



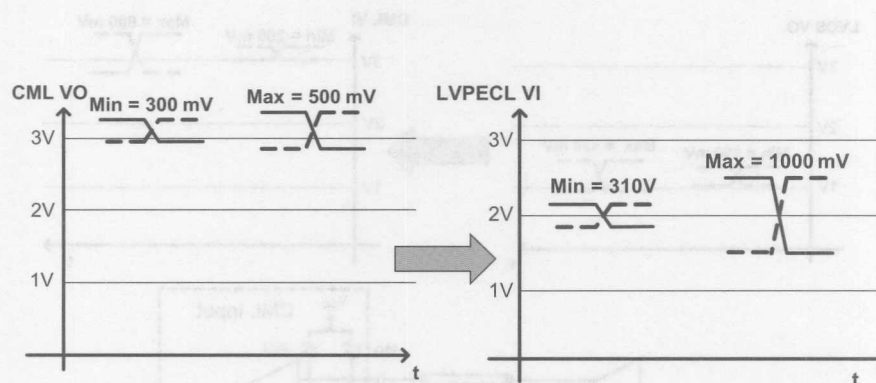
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Interfacing LVDS to CML interfaces is straightforward.

No external termination and biasing resistors are required because CML inputs typically provide the self-biased termination resistors.

CML-to-LVPECL Interfaces

AC Coupled (1 of 2)



Note: VO = Voltage output/VI = Voltage input



A CML-to-LVPECL interface is similar to a CM-to-LVDS interface.

CML-to-LVPECL Interfaces

AC Coupled (2 of 2)

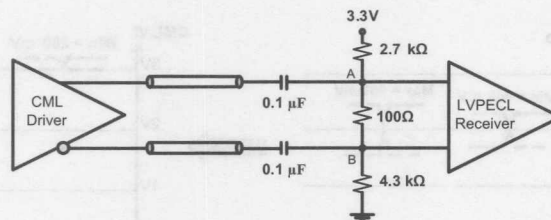


Figure (a)

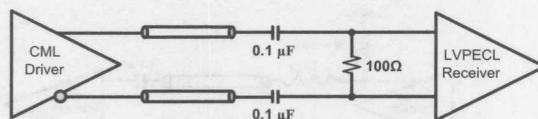


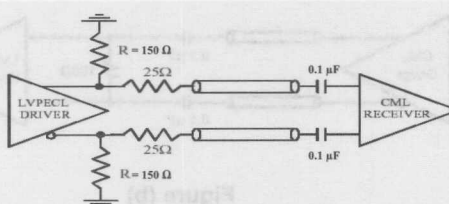
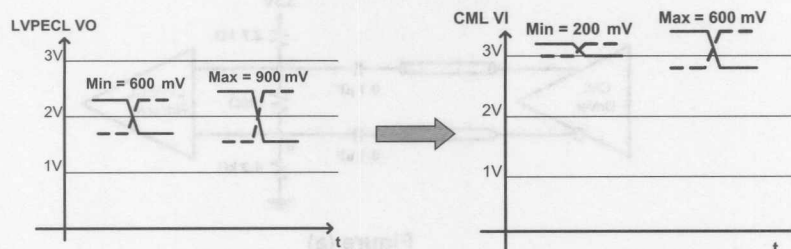
Figure (b)



The resistor network shown in Figure (a) provides a bias voltage (common-mode voltage) at 2V with a 100Ω termination. This configuration also provides failsafe biasing. Figure (b) shows the termination scheme if the LVPECL receiver input is internally biased.

LVPECL-to-CML Interfaces

AC Coupled



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When AC-coupling LVPECL-to-CML interfaces, designers should use an attenuator network. The MAX VOD for a LVPECL device will be much larger than the Max VID limit for a CML device. 25Ω series resistors can be used to provide an attenuation of 0.67.

LVPECL outputs need to be terminated to 150Ω to obtain the correct DC biasing.

Level Translation Summary

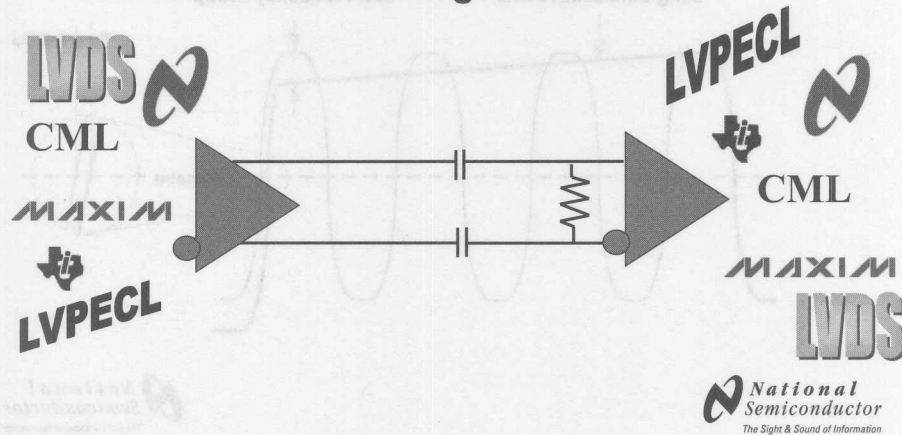
- For optimum performance with DC- and AC-coupled applications, the following should be considered:
 - Common-mode range
 - Offset voltage
 - Termination resistance
- AC coupling provides the simplest interface methodology with the fewest number of components. However, the following needs to be considered for AC-coupled applications:
 - Capacitor value selection
 - Data encoding



AC-Coupling Considerations

AC-Coupling Considerations

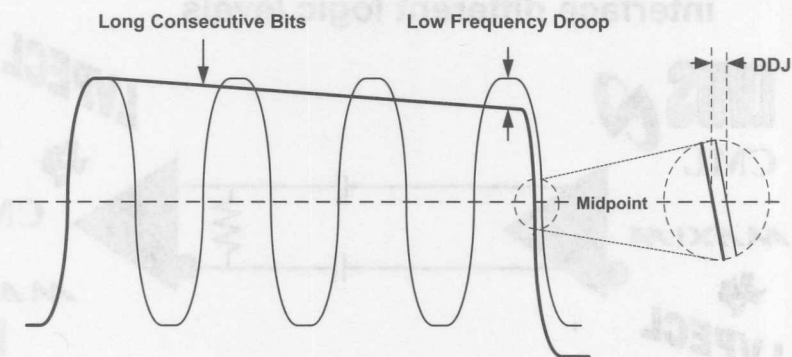
- AC-coupling provides the simplest interface method and requires the fewest amount of external components to interface different logic levels



Hardware manufacturers may not control both ends of a transmission link. AC-coupling allows them to make few assumptions about the driver or receiver they may be interfacing with.

Data-Dependent Jitter (DDJ)

- DDJ shifts crossing points, resulting in higher jitter and possible bit errors



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For AC-coupled applications, long strings of 1s or 0s cause a voltage droop to occur. This droop results in low-frequency, Data-Dependent Jitter (DDJ). Therefore, care should be placed on capacitor value selection.

Selecting Capacitor Values

- $C = (7.8 \times N \times T_b)/R$
 - T_b = bit period
 - R = impedance
 - N = the maximum number of consecutive identical bits
- Example:
 - 2.488 Gbps = 402 ps (T_b)
 - $R = 100\Omega$ (for LVDS devices)
 - $N = 100$ consecutive bits
$$C = (7.8 \times 100 \times 402 \text{ ps})/100\Omega$$

$$= 3.12 \text{ nF}$$
- Would recommend using a 0.1 μF or 0.01 μF capacitor



For a 2.488 Gbps receiver, $T_b = 402$ ps. If $N = 100$ bits and $R = 100\Omega$, the calculated C is 3.12 nF. Using a 0.01 μF for this scenario would suffice.

The most commonly used capacitor values found in high-speed applications are 0.1 μF and 0.01 μF capacitors. These capacitors are easy to find and have sufficient bandwidth to support most high-speed data rates.

When using AC-coupling capacitors, the smallest package size should always be chosen. This minimizes package parasitic effects on signal integrity.

Encoding Data

8-/10-bit Coding

Value (Decimal)	Value (Binary)	10-bit Code	Alternate Code
	HGF EDCBA	abcdei fghj	abcdei fghj
0	000 00000	100111 0100	011000 1011
1	000 00001	011011 0100	100010 1011
2	000 00010	101101 0100	010010 1011
3	000 00011	110001 1011	110001 0100
4	000 00100	110101 0100	001010 1011
5	000 00101	101001 1011	101001 0100
6	000 00110	011001 1011	011001 0100
7	000 00111	111000 1011	000111 0100
8	000 01000	111001 0100	000110 1011
9	000 01001	100101 1011	100101 0100
10	000 01010	010101 1011	010101 0100
⋮	⋮	⋮	⋮

Note – all codes are not 100% DC balanced, but the overall transmission is balanced

Max Run Length = 5

Running Disparity
(RD_{max}) = 3

Bandwidth cost = 20%



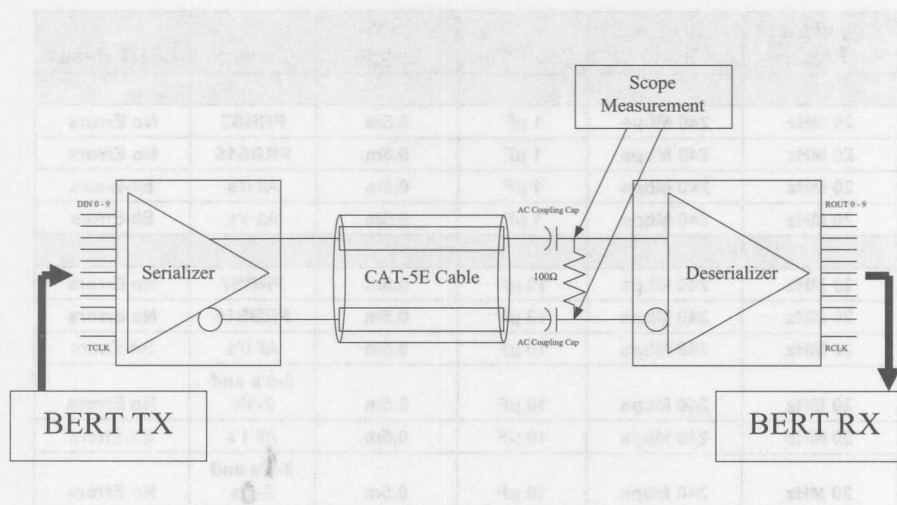
For AC-coupled applications, encoded data should be used. Encoding data that results in an equal number of 1s and 0s is commonly referred to as DC-balanced data. Although some AC-coupled applications may work without DC-balanced data, using encoded data optimizes performance and is strongly recommended.

One type of encoded data is 8-/10-bit coding. As you can see, each 8-bit binary value is translated into 2 possible 10-bit codes. A running tally is kept of the Running Disparity (RD) and the appropriate code selected to ensure a maximum RD of three. Run length is a maximum of five with this scheme, and the bandwidth penalty is 20%, 2 out of every 10 bits.

From a data validation perspective, this type of coding has an added benefit. With 8-/10-bit encoded data, there are only a certain number of valid codes – invalid codes represent a transmission error.

Other types of coding such as Manchester exist. However because of the popularity of 8-/10-bit encoded data, it was used for this example.

AC-Coupled Experiment



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An AC-coupled test setup with the 10-bit serializer (DS92LV1021A) and deserializer (DS92LV1212A) were used to make some measurements. A Tektronix MB100 BERT was used to validate data integrity.

Evaluation Results

Input Clk Freq.	Line Data Rate	Cap Value	Cable Length	Pattern	BERT Result
20 MHz	240 Mbps	1 μ F	0.5m	PRBS7	No Errors
20 MHz	240 Mbps	1 μ F	0.5m	PRBS15	No Errors
20 MHz	240 Mbps	1 μ F	0.5m	All 0's	Bit-Errors
20 MHz	240 Mbps	1 μ F	0.5m	All 1's	Bit-Errors
20 MHz	240 Mbps	10 μ F	0.5m	PRBS7	No Errors
20 MHz	240 Mbps	10 μ F	0.5m	PRBS15	No Errors
20 MHz	240 Mbps	10 μ F	0.5m	All 0's	Bit-Errors
20 MHz	240 Mbps	10 μ F	0.5m	8-0's and 2-1's	No Errors
20 MHz	240 Mbps	10 μ F	0.5m	All 1's	Bit-Errors
20 MHz	240 Mbps	10 μ F	0.5m	8-1's and 2-0's	No Errors



At 20 MHz, a string of all 1s or all 0s was the only pattern which caused bit errors. In the next few slides, we will discuss the relationship between coded data and bit errors.

Evaluation Summary

- When AC coupling, long strings of consecutive 0s and 1s shift the common-mode voltage and reduce noise margin
- At 20 MHz with a 0.5m cable and a capacitor value of 10 μ F, bit-errors occur for an all 0 or all 1 pattern
- Under the same test conditions, the maximum number of consecutive identical bits allowed for error-free operation was 8 bits (8 0s or 8 1s)
- Under the same test conditions and a PRBS pattern, the link is error-free for both 0.1 and 10 μ F capacitor values

NOTE: All consecutive high bits were placed starting from the first data bit (DIN0), and all low bits were placed starting from the last data bit closest to the CLK0 bit

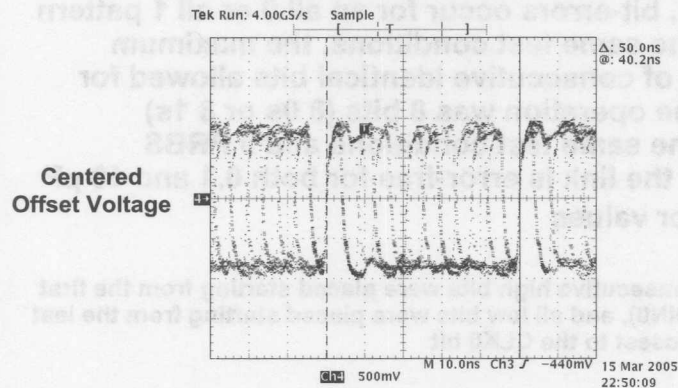


Error-Free Differential Signal

Transition rich pattern

Cable Length: 0.5m/20 MHz/PRBS-15/Capacitor Value = 10 μ F

NOTE: measured with a differential probe



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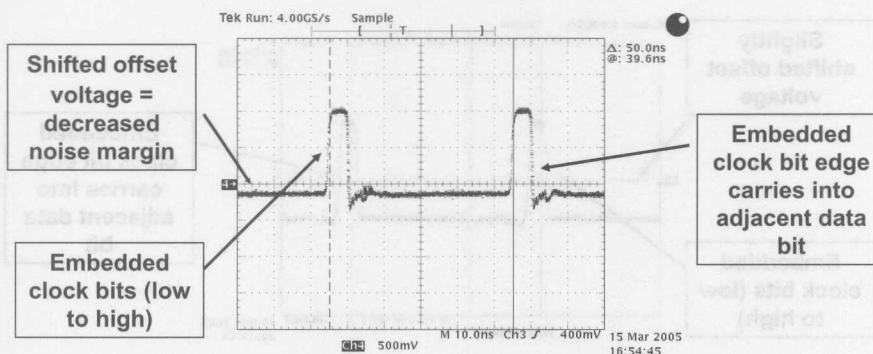
Diff probe
loses CM.

Failing Differential Signal

Bit Errors Reported - 1 μ F Capacitor

Cable length: 0.5m/20 MHz/All 0 pattern/Capacitor value = 1 μ F

NOTE: measured with a differential probe



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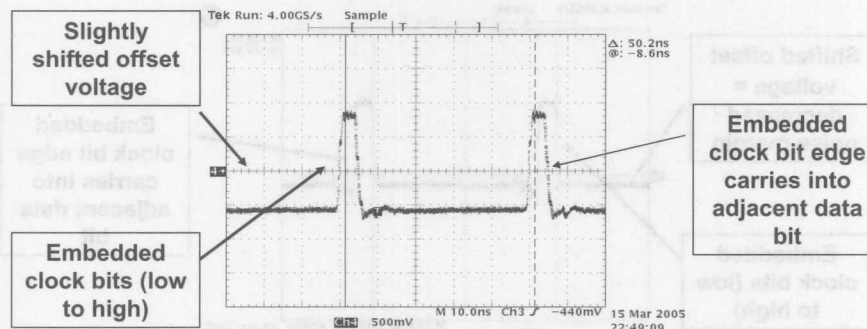
Here is an example with our DS90LV1021A and DS90LV1212A start/stop bit SerDes. As shown above, the data arriving at the Rx is a completely unbalanced long run of consecutive 0s. Because these devices contain embedded clock bits (a single 1 and 0 representing a clock), every 12 bits transmitted contain 10 databits and two clock bits. Long strings of consecutive 1s or 0s will result in the common-mode voltage shifting in a linear fashion, and consequently, the noise margin will be reduced to a fraction on the nominal. Typically, LVDS receivers call for a ± 100 mV threshold. In this scope shot, there is only approximately 75 mV of noise margin.

Failing Differential Signal

Bit Errors Reported - 10 μ F Capacitor

Cable length: 0.5m/20 MHz/All 0 pattern/Capacitor value = 10 μ F

NOTE: measured with a differential probe

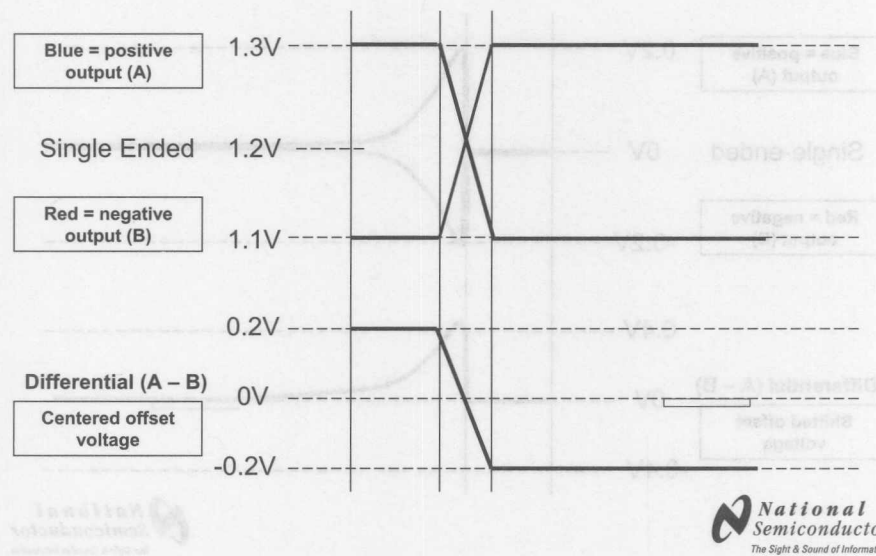


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With a 10 μ F capacitor, there is only a slight shift in offset voltage. Using the larger capacitor value provides more noise margin.

Typical Offset Voltage

DC-Coupled Applications

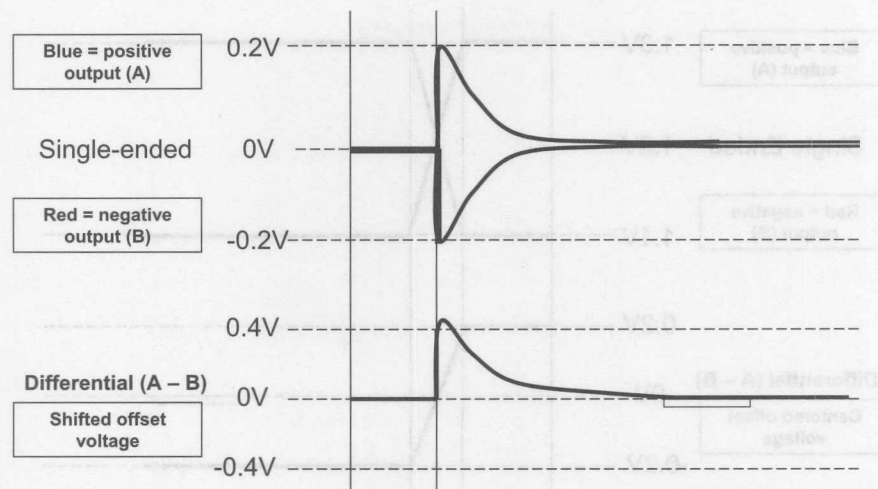


The graphic shown above is representative of the embedded clock bits from the DS92LV1021A transmitter and all 0s data bits.

For AC-coupled applications, over time, the DC component of the signal is removed and the common-mode voltage drifts to 0V. This results in a shifted DC offset voltage in the differential signal and reduces noise margin.

Shifted Offset Voltage

AC-Coupled Applications

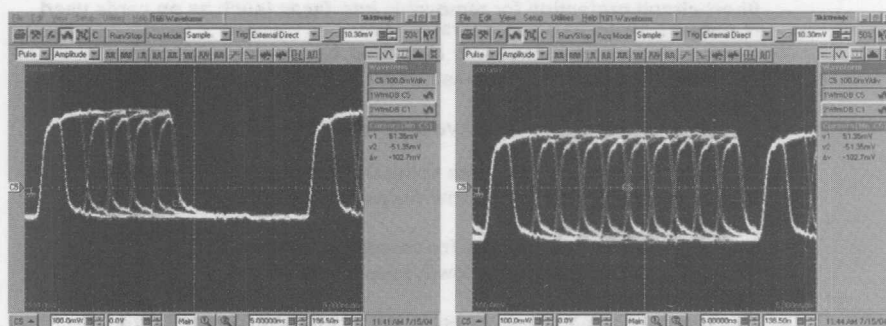


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The graphic shown above is representative of the embedded clock bits from the DS92LV1021A transmitter and all 0s data bits.

For AC-coupled applications, over time, the DC component of the signal is removed and the common-mode voltage drifts to 0V. This results in a shifted DC offset voltage in the differential signal and reduces noise margin.

Restored Offset Voltage



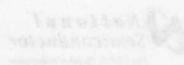
Increased number of switching bits
restores proper offset voltage



Unlike the previous all 0s case with embedded clock bits from the DS92LV1021A, the above scope shots show that increasing the number of switching bits restores the proper offset voltage. As more bits begin switching, the DC offset voltage is restored and the signals are less likely to decay to 0V. This results in more differential swing and more noise margin.

Conclusions

- AC-coupled advantages:
 - Simplest method to interface different technologies
 - Fewest number of components required to restore DC offset voltages
 - Short-circuit protection for removable interfaces (such as on cards used in network switches and routers)
 - Controls DC offset voltages for long-haul, box-to-box applications
 - AC droop in signals can increase jitter
- AC-coupled limitations:
 - May need to restore DC offset voltage when internal biasing is not provided
 - Optimum performance requires using DC-balanced data
 - May be bandwidth limited for low-frequency data rates
- DC-coupled advantages:
 - No droop/best signal integrity for compatible interfaces
 - No bandwidth limitations for low-frequency data rates
- DC-coupled limitations:
 - May require complex resistor networks when using devices with different interface technologies
 - Possible DC offset voltage drift for long-haul, box-to-box applications



By using AC coupling, many different interfaces can be used together. Additionally, using AC-coupled resistor networks can provide more noise margin than a DC-coupled implementation when encoded data is used.

Interface WEBENCH® Online Tools

One of the many tools a system engineer must incorporate is to select the correct interface product based on parameters such as data rate, channel length, and jitter margin. National has simplified this selection process by providing Web tools like the Interface Product Finder along with Interface WEBENCH® online tools.

To begin, go to www.national.com. The task of configuring signal integrity can be accomplished in three easy steps.

In the first step, enter in your design LVDS requirements and click on recommended parts to see your results.

STEP 1: Define Your LVDS Requirements

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Innovative Products from
the LVDS Pioneer and Leader

[Select](#) | [Design](#) | [Buy](#) | [Explore](#) | [Contact Us](#) | [Analog University®](#) | [WEBENCH® Tools](#) | [My Profile](#)

[Sign-Off](#) | [日本語](#) | [简体中文](#) | [繁體中文](#) | [한국어](#)

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LVDS.NATIONAL.COM

Select

Select your LVDS device based on device function, data rate, etc

Click on recommended parts to see results

Design

Interface Product Finder

Device Function: help

Data Rate >=: Mbps help

Input Type: help

Number of Inputs: help

Output Type: help

Number of Outputs: help

Supply Voltage: ☐ 3.3V or less ☐ 5V help

→ RECOMMENDED PARTS

Explore

What's New:
Interface Products Selection Guide for Q1 of 2006 (pdf 3.0MB)

DS25MB200
Dual 2.5 Gb/s 1:2 Mux/Buffer with Input Equalization and Output Pre-Emphasis

DS90LV011AH, DS90LV012AH, DS90LV027AH, DS90LV028AH, DS90LV049H
High Temperature LVDS Drivers and Receivers

DS42MB200T
Dual 4.25 Gb/s 1:2 Mux/Buffer with Input Equalization and Output Pre-Emphasis

DS40MB200
Dual 4 Gb/s 1:2 Mux/Buffer with Input Equalization and Output Pre-Emphasis

DS15MB200
Dual 1.5 Gbps LVDS 1:2/2:1 Mux/Buffer with Pre-emphasis

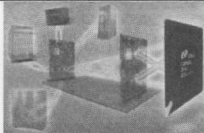


One of the many tasks a system engineer must accomplish is to select the correct interface product based on parameters such as data rates, channel length, and jitter margin. National has simplified this selection process by providing Web tools like the Interface Product Finder along with Interface WEBENCH® online tools.

To begin, go to LVDS.NATIONAL.COM. The task of evaluating signal integrity can be accomplished in three easy steps.

In the first step, enter in your desired LVDS requirements and click on recommended parts to see your results.






STEP 2: Select Your LVDS Product













Required Parameters

Device Function	Mux-Buffer
Data Rate >=	2000 Mbps
Input Type	All
Number of Inputs	1
Output Type	All
Number of Outputs	1

Recommended Parts

 Product Folder
  Datasheet
  24 Hour Samples
  Samples
  Buy Now

NOTE: An attribute highlighted in RED indicates that this product is not a direct match.

Part Number	Pkg	Function	Payload per Channel (Mbps)	Total Throughput (Mbps)	Supply Voltage	Number of Inputs	Input Compatibility	Number of Outputs	Output Compatibility	Score	Select
		↓↑	↓↑	↓↑	↓↑	↓↑	↓↑	↓↑	↓↑	↓↑	
DS25MB200		Mux-Buffer	2500	2500	3.3	6	LVDS/LVPECL/CML	6	CML	146.04	   
DS40MB200		Mux-Buffer	4000	4000	3.3	6	LVDS/LVPECL/CML	6	CML	131.66	   

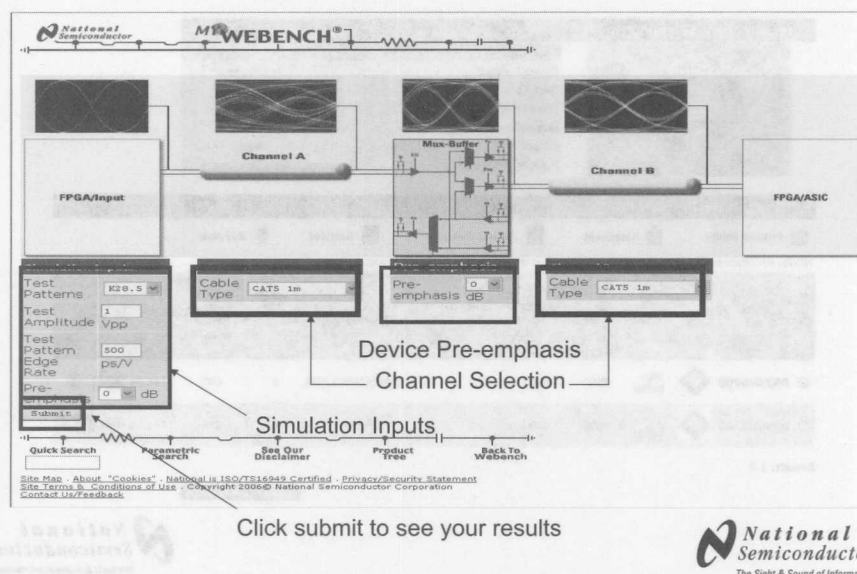
Results: 1-2

[→ CREATE A DESIGN](#)



In Step 2, the Interface Product Finder will select several appropriate devices that meet or beat your stated criteria in Step 1. Select the part that best fit your desired requirements. Proceed by clicking on "Create a Design" to simulate your selected devices.

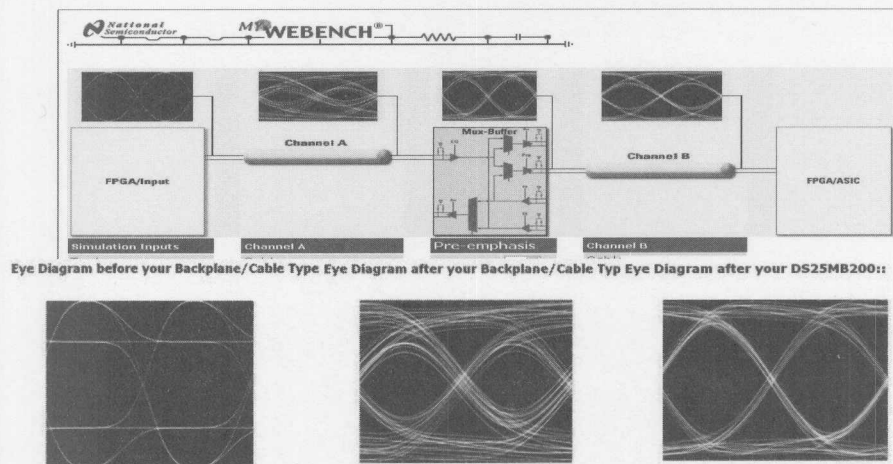
STEP 3: Simulate Your LVDS Product



Click submit to see your results

Once you have selected your part, you can simulate it with a variety of channel types and simulation inputs. Some available channel types include CAT-5, CAT-6, and FR4 traces. Simulation inputs will include parameters such as test patterns, test amplitude, and pre-emphasis. Additionally, pre-emphasis for the device can also be adjusted, if needed. Finally, click the submit button to see your results.

Results for Your LVDS Product



The last step would be the displaying of your results. Here you can see how the eye diagram is affected by channels and devices you have selected. By looking at the eye diagrams, the engineer will have a very good indicator of the feasibility and integrity of their simulated system.

Results for Your LVDS Product



www.microware.com

The last step would be the display of your results. Here you can see how the system is affected by channel and device you have selected. By looking at the eye diagram, the system will have a very good indication of the feasibility and integrity of their signal system.

Using Mux-Buffers

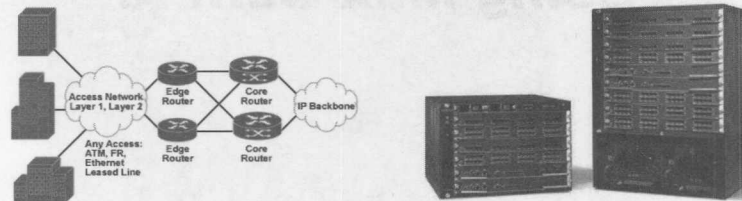
In this section we will discuss National's mux-buffer and signal-conditioning parts, their applications, the internal architecture, and related parts in the product family.

The first application to cover is "redundancy."

National's Mux-Buffer Signal-Conditioning Parts

Network switches, edge aggregation router, and core router applications

- The enterprise equipment is mostly chassis based
- Mux-buffer can reduce network down time by providing redundancy in the equipment



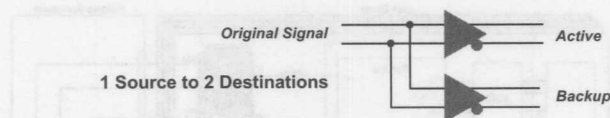
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Most of the enterprise network switches, edge aggregation routers, and core routers are chassis based. With a modular system, redundancy is easily built in using National multiplexer and buffer (mux-buffer) parts.

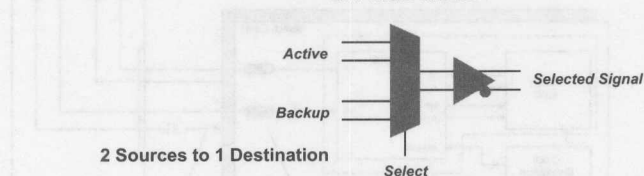
The benefit of having redundancy is to reduce network down time.

Examples for Redundancy

1:2 Splitter Mode



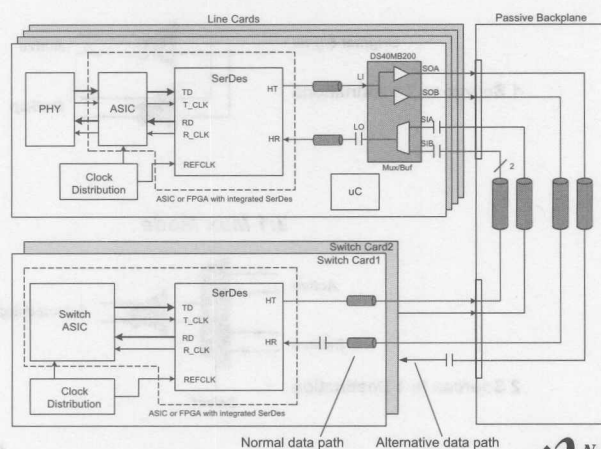
2:1 Mux Mode



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This shows the internal structure of a mux-buffer. The buffer splits incoming data into two paths, and the mux (multiplexer) selects which data source to send to the output.

Redundancy in Switch Cards

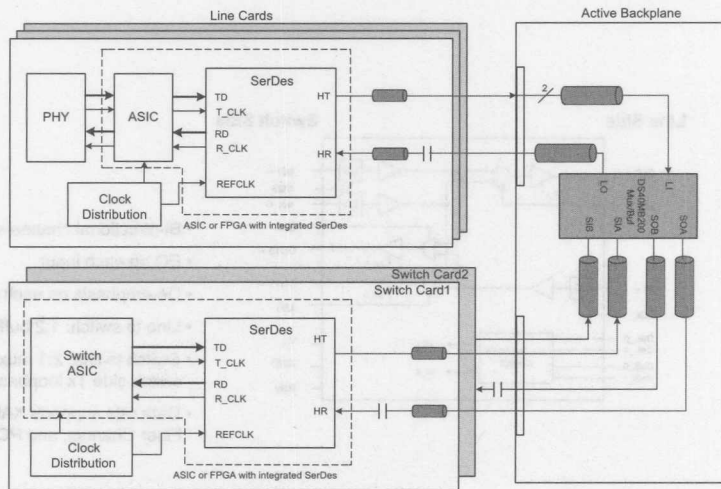


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In a network switch chassis environment, the mux-buffer can create data-path redundancy. If one switch card fails, the on-board management controller can switch the data path to a backup switch card. This redundancy allows minimum network down time.

The diagram shows a passive backplane configuration and the mux-buffer is located on each of the line cards.

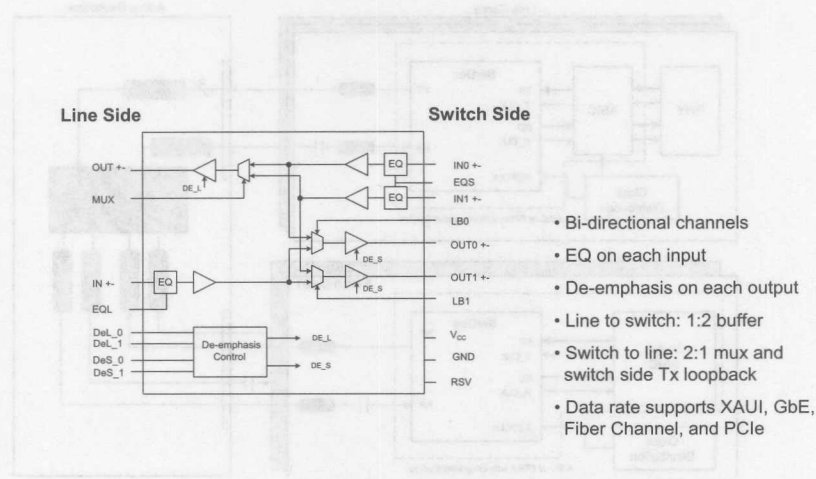
Redundancy in Switch Cards



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The mux-buffer also can be located on the backplane, making this chassis an active backplane.

Typical Mux-Buffer Internal Architecture

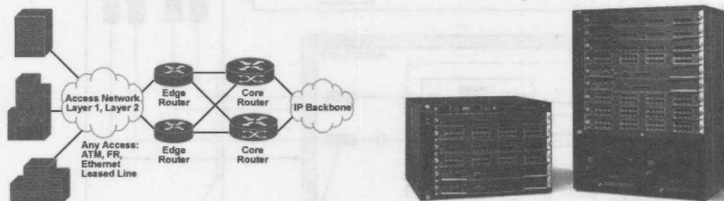


The typical mux-buffer component not only contains a mux and splitters, but it also may contain signal-conditioning functions on its output and its input.

National's Mux-Buffer Signal-Conditioning Parts

Network switches, edge aggregation router, and core router applications

- 1 G to 3.125 Gbps backplane interface applications and conform to XAUI jitter tolerance. Many networking backplanes are based on XAUI-like protocols
- Trends: Higher-speed line cards are needed to handle faster wire speeds (e.g., OC-48, OC-192, 10 GbE) and more complex multi-services. This means higher backplane speed

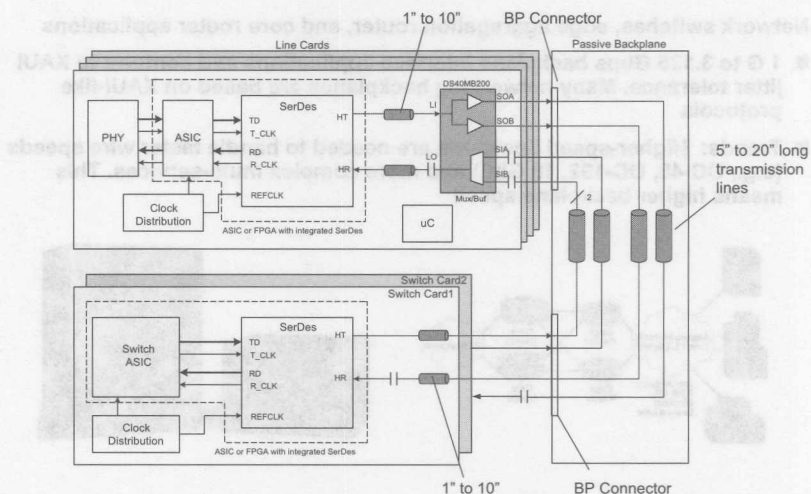


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Why build signal conditioning into the mux-buffer parts? Let's take a look at where signal-conditioning parts are used.

The enterprise network switches and routers are chassis based. With such a modularized system, the signal normally travels from one card to another card via a long signal path.

Signal-Conditioning Features



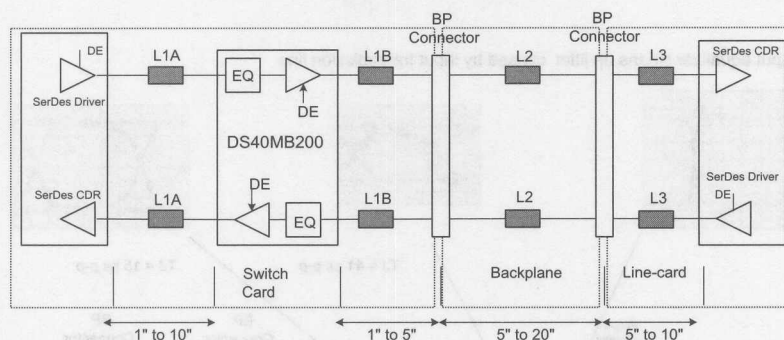
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In this example, the source signal would start from an ASIC or FPGA, then pass through a 1" to 10" circuit board trace, a backplane connector, 5" to 20" backplane cabling, another backplane connector, and through another 1" to 10" circuit board trace to the final destination.

Because of dielectric loss and skin effect, there will be attenuation to the high-frequency signal band. This attenuation can create data-dependent jitter and cause data errors at the receiving end.

By applying National signal-conditioning parts near the backplane connector, the signal is conditioned going out to the backplane and coming in from the backplane, reducing jitter and reducing error.

Signal-Conditioning Features



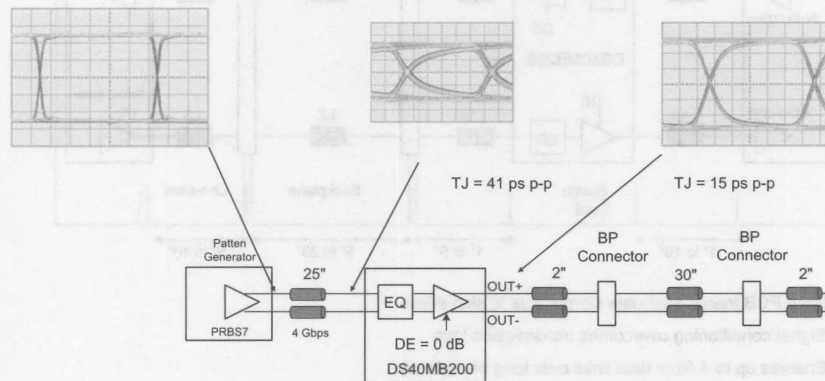
- Long PCB traces attenuate signals due to skin effect
- Signal conditioning overcomes transmission loss
- Enables up to 4 Gb/s data links over long backplanes



Compared to the previous slide, the signal-conditioning part not only recovers signal loss across the board traces, but also conditions the signal in both transmitting and receiving directions. This is achieved by equalizing the signal, as shown in the next slide.

Input Equalizer

- Input equalizer cleans up jitter caused by input transmission line



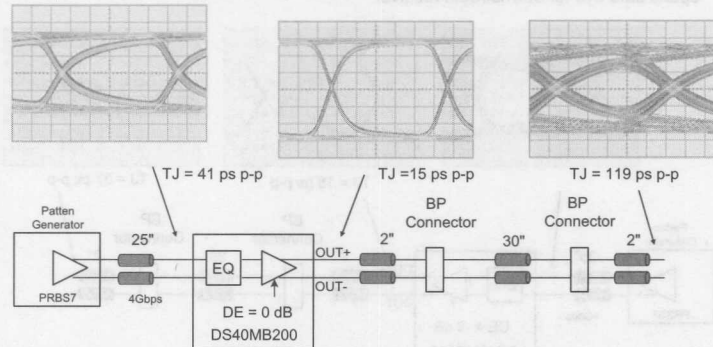
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On the receiving end, there is an equalizer. The equalizer boosts the high-frequency signals to compensate for the loss due to skin effect and dielectric.

The center trace shows the jitter in the signal after a 25" board trace. The resulting signal at the output has restored amplitude and reduced jitter.

Output De-emphasis OFF

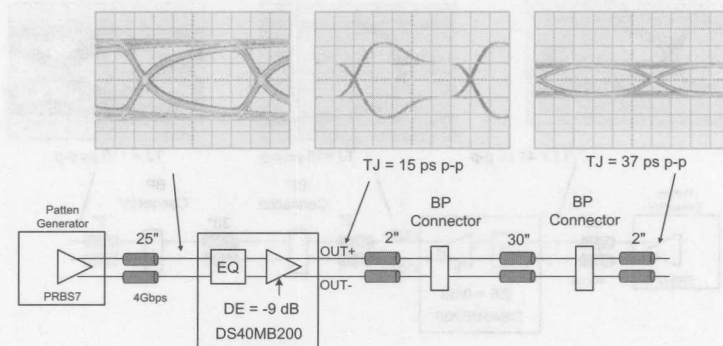
- Driver output with no de-emphasis – eye starts to close at the end of the transmission line



After equalization, the jitter is reduced. On the transmitting side, after 32" of board trace and two backplane connectors, the signal amplitude again reduces and the jitter increases.

Output De-emphasis ON

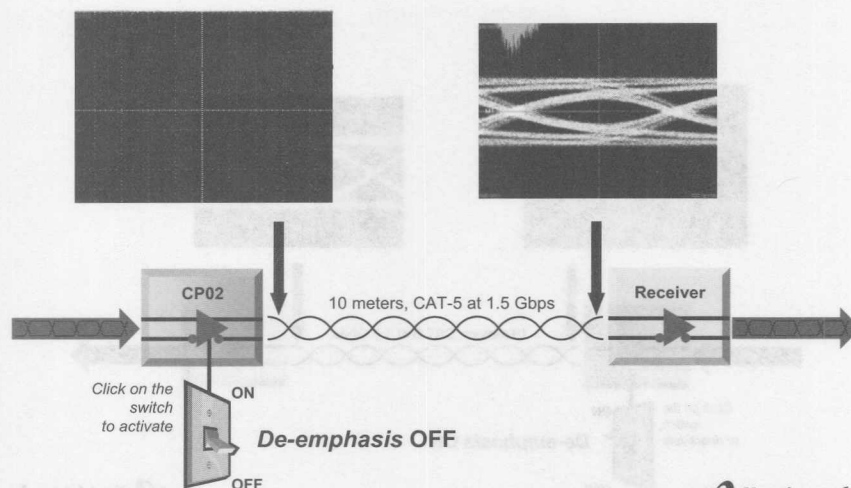
- Driver de-emphasis equalizes long transmission line - reduces jitter and opens data eye for downstream receiver



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By turning on the de-emphasis at the transmitter output, the low-frequency component of the signal is attenuated relative to the high-frequency component, and the resulting signal at the end of transmission line is a low jitter signal. Note that the final signal amplitude is reduced.

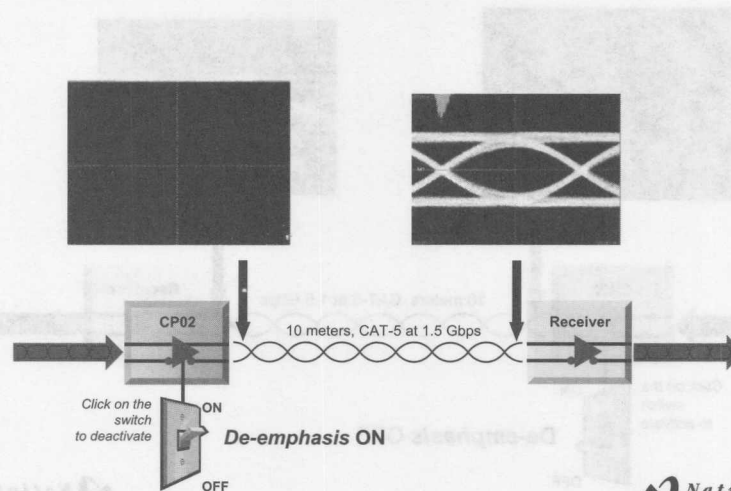
How De-emphasis Works



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Here is another demonstration of the de-emphasis. By clicking on the switch, the de-emphasis can be turned on/off. The jitter histogram shows reduced jitter.

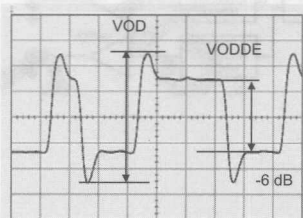
How De-emphasis Works



Lower jitter is achieved through de-emphasis. This demo is using the National cross point switch.

Adjustable De-emphasis Steps

DE [1:0]	VOD (mV)	VODDE (mV)	VODDE in dB
0 0	1200	1200	0
0 1	1200	850	-3
1 0	1200	600	-6
1 1	1200	426	-9

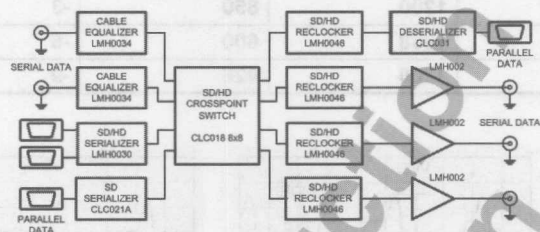


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On many of the National parts, the de-emphasis level is adjustable. This specific example shows there are four levels of de-emphasis to match the transmission channel attenuation, i.e., different PCB trace length or cable length.

Redundancy in SDV

Serial Digital Video – Cross point switch; mux; repeater



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Mux-buffers and cross point switches are similar. A cross point switch output can select any input and an input can go to multiple outputs.

In addition to enterprise network switch and routers, the mux-buffer and cross point switch can be used in Serial Digital Video (SDV) applications.

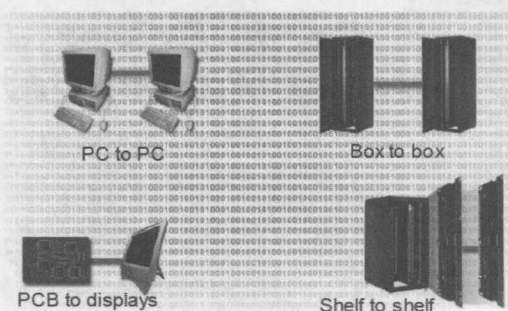
The block diagram illustrates the function of multiplexing and switching.

Cable Driver Using Mux-Buffer

The mux-buffer signal-conditioning parts also can be used as cable drivers.

DS40MB200 as a Cable Driver

- PCI express, SATA, XAUI, Infiniband, etc. are used to link between systems and computers. The bit rate can reach beyond 1 Gbps
- High speed cabling requires signal conditioning to overcome transmission loss
- DS40MB200 is used as an example that can be used to improve signal quality over cable so that receive can recover transmitted signal
- Applications – Network inter-system connection, storage device attachment, computer-to-computer connection, board-to-board connection, etc

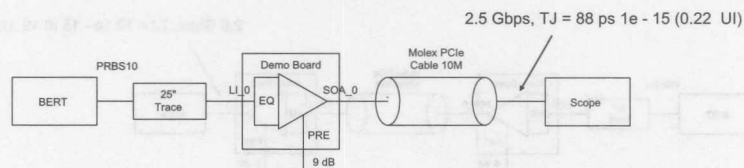
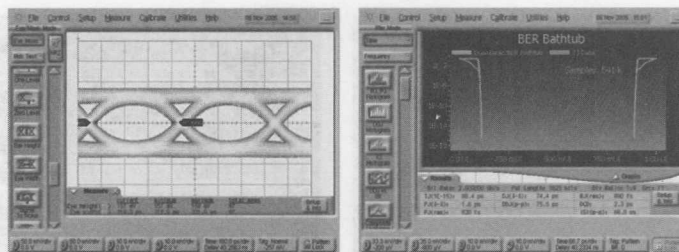


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The ever-increasing communication data rate has created higher demands on signal-conditioning parts used to drive cables. Standards such as PCI Express, Serial ATA, XAUI, and Infiniband are used to link communications between the systems.

The applications are Storage Area Network (SAN), digital cable connecting computer to display, personal computer to personal computer, personal computer to peripheral devices, chassis systems to chassis systems, etc.

PCI Express Cable Example

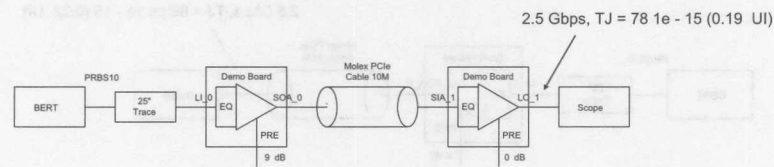
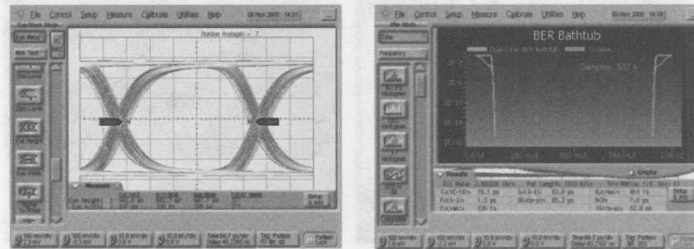


- 2.5 Gbps, with DS25MB200 on driver sides of the cable



This slide shows the DS40MB200 is capable of driving 10 meters of PCI Express cable. With the output de-emphasis turned on, the signal at the destination has less than 0.22 UI of jitter.

PCI Express Cable Example



• 2.5 Gbps, with DS25MB200 on both sides of the cable

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With signal conditioning on both sides of the cable, de-emphasis on the transmitting end, and equalization on the receiving end, the jitter is reduced from 0.22 UI to 0.19 UI.

1
unit
1/F

The Mux-Buffer and Signal-Conditioning Family

- DS40MB200 – 4.00 Gbps; Dual-channel; 1:2 buf; 2:1 mux; De-emp; EQ
- DS42MB200 – 4.25 Gbps; Dual-channel; Ind temp; 1:2 buf; 2:1 mux; De-emp; EQ
- DS25MB200 – 2.5 Gbps; Dual channel; 1:2 buffer; 2:1 mux; De-emp; EQ;
- DS15MB200 – 1.5 Gbps; Dual channel; 1:2 buffer; 2:1 mux; De-emp
- SCAN15MB200 – 1.5 Gbps; Dual channel; 1:2 buffer; 2:1 mux; JTAG
- DS90LV004 – 1.5 Gbps; Quad channel; Buffer; Pre-emphasis
- SCAN90004 – 1.5 Gbps; Quad channel; Buffer; Pre-emphasis; JTAG
- DS42BR400 – 4.25 GbpsQ transceiver
- EQ50F100 – 6.25 Gbps; Backplane equalizer
- DS90CP04 – 2.5 Gbps; 4x4 crosspoint switch
- SCAN90CP02 – 1.5 Gbps; 2x2 crosspoint switch with Pre-emphasis; JTAG
- DS90CP22 – 0.8 Gbps; 2x2 crosspoint switch
- CLC018 – 1.5 Gbps; 8x8 crosspoint switch



For detailed information on applications, part selection, and part descriptions, please refer to the Interface Product Selection Guide and Broadcast Video Selection Guide.

The component information such as datasheet, reference design, evaluation kit, and white paper is also available at <http://lvds.national.com>.

Cable Driving

There are several major types of cable, each with many variations to cover specific conditions in bandwidth requirements.

Coaxial: This is the highest-bandwidth electrical cable. By definition, it is fully shielded and also offers high bandwidth, low-loss transmission. Coaxial connectors are commonly used in CATV and Twisted Pair. This common cable type is most often seen in Ethernet applications in CAT-5 or CAT-6 four-pair configurations. The widespread use also makes it a relatively low cost solution. It can also be found in many other low-to-medium speed applications where signal-to-noise ratio or timing is not critical or the distance is short.

Twisted-pair: This type of cable represents a "middle ground" between the low-loss coaxial cable and the economical twisted pair cable. It is used for high-speed serial specifications like InfiniBand.

Fiber Optic: When signals need to travel very long distances, fiber optics are often used. Fiber optic cables represent the lowest-loss medium possible for serial communications. It is necessary to do an electrical-to-optical conversion which adds to the overall cost. This additional cost limits the adoption of fiber in applications that electrical cables can accomplish with the help of signal conditioning.

Cable Types

- **Coaxial**
 - For the highest bandwidth and longest drive distance
 - Used often in video broadcast equipment
- **Twisted Pair**
 - For economical data transfer
 - CAT-5, CAT-6, CAT-7
 - Specialty connectors are eliminating RJ45 crosstalk
- **Twin-axial**
 - Used for high-density, high-bandwidth applications
 - Seen as a standard cable for specifications like Infiniband
- **Fiber Optic**
 - Used for extreme distance and bandwidth
 - Intra campus to intercity applications



There are several major types of cable, each with many variations to cover specific conditions or bandwidth requirements.

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Signal-Conditioning Options

- De-emphasis/pre-emphasis
 - Output compensation to adjust for transmission loss
- Fixed/adaptive equalization
 - Input compensation to adjust for transmission loss
- Multilevel signaling
 - Improved utilization of transmission line bandwidth



There are three options for signal conditioning. The first two are the most common and available from multiple silicon sources.

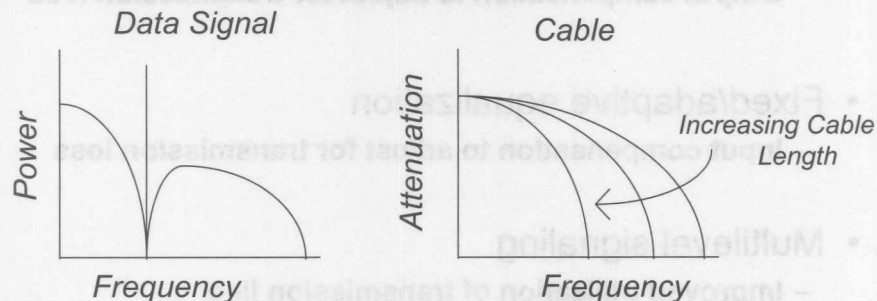
De-emphasis/pre-emphasis: Either of these terms can generally be used to define an output signal-conditioning technique to increase the high-frequency energy of a data signal at the driving device. This is done in anticipation of the losses that will be found in the transmission path.

Fixed/adaptive equalization: Input equalization is the use of a high-pass filter that is the complement to the low-pass characteristic of the cable that you are using. This helps to compensate for some of the attenuation effects of the cable.

Multilevel signaling: This technique uses four or more signal levels to compress more data into a lower frequency range. Reducing the maximum frequency of interest allows data to be transferred longer distances or at higher speeds relative to normal two-state digital data.

Characteristics of Serial Data

- **Attenuation and bandwidth**



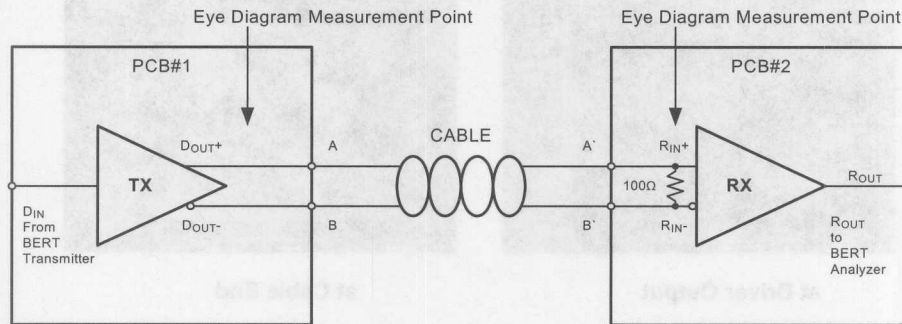
Frequency Domain Representation



Looking at any serial data signal with a spectrum analyzer will give the picture on the left. If the data rate is 1 Gbps, then the first notch in the pattern will be at 1 GHz. More notches will be present at multiples of the first notch seen. In this case, they would be seen at 2 GHz, 3 GHz, 4 GHz, etc.

The cables used for transmission always will show increasing levels of attenuation for longer lengths.

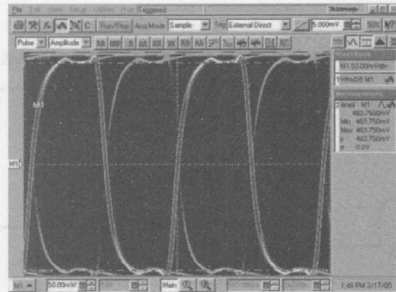
Cable Driving



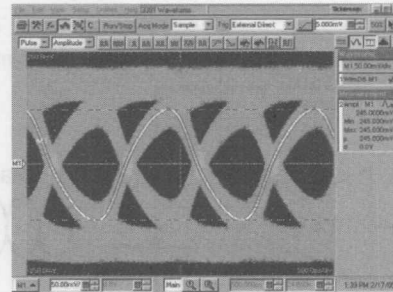
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The cable drive set up includes both a transmitter and receiver. The topology is point to point. The waveforms are taken at the driver output and the receiver input. The signal quality of the receiver output is also analyzed to ensure robust reception of the attenuated signal.

Cable Loss Example



at Driver Output



at Cable End

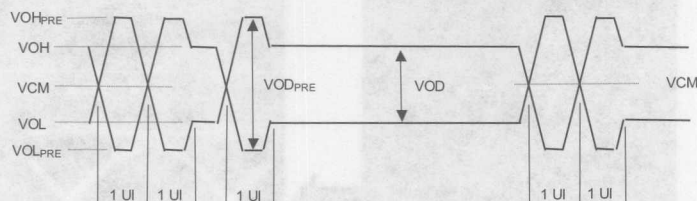
CAT-6 Cable loss of 0.4 dB/meter at 400 MHz
– 6 dB or 50% reduction after 15m



These graphics show the same signal, one at the beginning of the cable and the other at the end. The highest-frequency signal at the end of the cable shows a 6 dB or 50% reduction in amplitude.

Pre-Emphasis Example DS15MB200 and DS90LV004

- De-emphasis/pre-emphasis
 - Output compensation to adjust for transmission loss

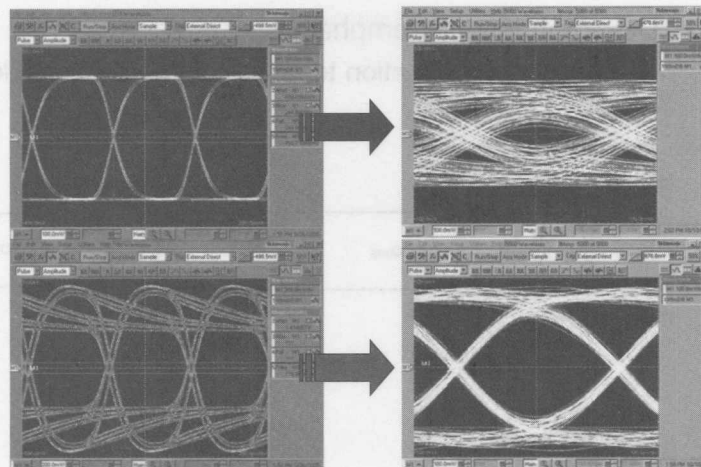


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The primary signal-conditioning technique used to improve LVDS performance is output pre-emphasis. Pre-emphasis is controlled amplitude and duration output overdrive used to compensate for high-frequency losses and extend transmission distance over cables and backplanes. The simplest and most effective pre-emphasis scheme is full-first-bit pre-emphasis.

The waveforms on the right show the difference between no pre-emphasis and 6 dB of pre-emphasis. The pre-emphasis boost cleans up the jitter seen at the input of the receiving device, extending the length of cable that can be driven at a given frequency.

Pre-Emphasis Example DS15MB200 and DS90LV004

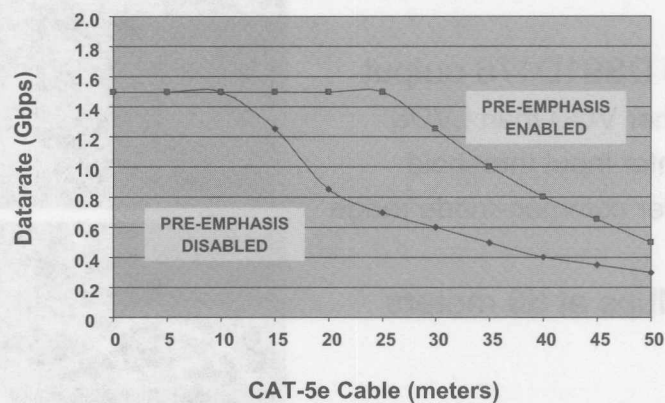


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The waveforms on the right show the difference between no pre-emphasis and 6 dB of pre-emphasis. The pre-emphasis boost cleans up the jitter seen at the input of the receiving device, extending the length of cable that can be driven at a given frequency.

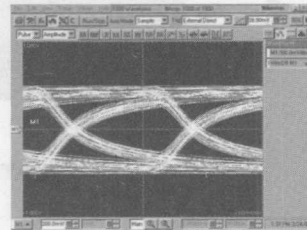
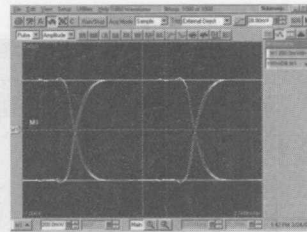
LVDS Cable Driving DS15MB200 and DS90LV004



Enabling pre-emphasis makes a significant improvement in driving distance and cable throughput.

M-LVDS Cable Driving

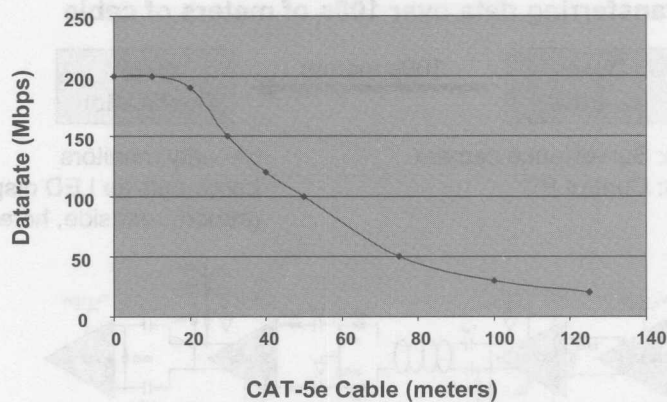
- At the DS91D176 output
 - Higher VOD than LVDS
 - Tighter input threshold
 - Wider common-mode range
- 100 Mbps at 50 meters



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While TIA/EIA-485 is better suited for longer-distance applications, M-LVDS provides true multi-point solutions with less power usage at greater speeds. The lower operating voltages of M-LVDS are the reason for the lower power consumption, but also the reason for the restriction to shorter distances where noise coupling and differential attenuation through the interconnect media are lower.

M-LVDS Cable Driving

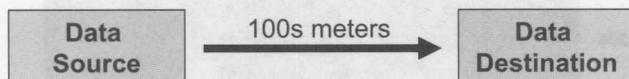


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The larger VOD, tighter input thresholds, and wider common-mode range of M-LVDS devices make them great candidates for driving significant distances over cable. In this example, the M-LVDS can achieve its full operation data rate across 20 meters of cable. At slower data rates, similar to RS485, the M-LVDS devices can transmit and receive data at distances of over 100 meters.

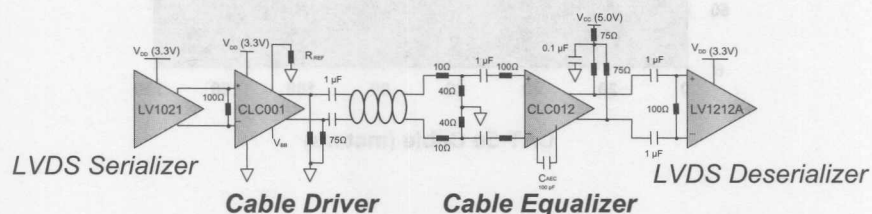
Adaptive Equalization

Transferring data over 100s of meters of cable



Example A: Surveillance camera
Example B: Control PC

Security monitors
Large outside LED display
(airport, roadside, hotel...)

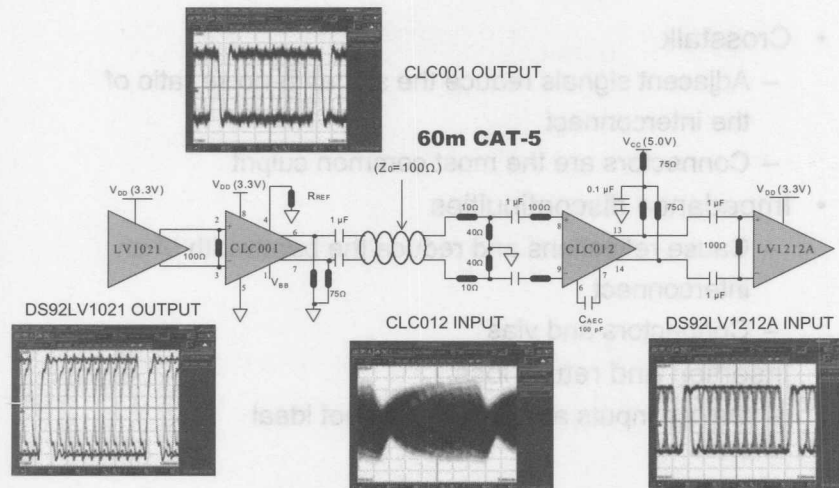


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National has many SDV products for the broadcast video professional equipment market. These products go into the studios that produce, edit, and distribute the digital video for broadcasting, closed circuit TV, and video on demand.

These same parts have applications in the broad market transferring data of any type. For example, the standard-definition digital TV cable drivers, retimers, and equalizers operate at 155 Mbps, which is the STM-1 telecom standard used through out the telecom world. Telecom OEMs use these SDV products in their equipment for sending the STM-1 data over many meters of cable. The SDV products also will work at the 622 Mbps data rate used in telecom applications.

Adaptive EQ Waveforms



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The CLC012 from National has the capability to equalize up to 300 meters of 75Ω Belden coaxial cable or 100 meters of common CAT-5e cable. It is important to take extra care when dealing with Twisted Pair (TP) cable. The high-gain amplifiers in the CLC012 will not be able to discriminate from excessive crosstalk and the small remaining signal from the distant transmitter. For this reason, it is recommended that shielded TP be used whenever possible and the unused pairs in the cable be terminated with 100Ω resistors.

It's Not Just Attenuation

Cable Drive Summary

- Crosstalk
 - Adjacent signals reduce the signal-to-noise ratio of the interconnect
 - Connectors are the most common culprit
- Impedance discontinuities
 - Cause reflections and reduce the bandwidth of an interconnect
 - Connectors and vias
- Insertion and return loss
 - Device inputs and outputs are not ideal

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Crosstalk cannot be forgotten and becomes increasingly important as the speeds increase into the Gbps range. Crosstalk is a concern for multi-conductor or multi-pair cables that do not have a good isolation between data carrying channels. In addition, connectors can be a significant source of loss induced by cross talk in a cable assembly. The conducting elements inside a connector radiate electromagnetic fields, which are coupled to the conductors in the adjacent pairs of the connector. Similar coupling occurs in the cylindrical vias used by adjacent connector pairs in a PCB. Consider a bi-directional signal transmission over a multi-channel cable where the drivers are driving at their full amplitude, and the receivers are receiving weak signals from their far-end partners, heavily attenuated by the cable's transmission loss. The near-end-crosstalk from the strong local driver, superimposed onto the weak receive signal, results in a poor signal-to-noise ratio. Neither driver pre-emphasis nor receiver equalization compensate for crosstalk; therefore, the designer should minimize crosstalk by selecting individual pair cable shielding and low crosstalk connectors when multi-channel data transmission is required.

Also, device inputs and outputs do not represent ideal sources or terminations. This non ideality allows energy from crosstalk and impedance discontinuities to be partially reflected at device inputs and outputs increasing the jitter on the primary signal.

As data speeds increase to and beyond 2 Gbps it is recommended that designers look to CML devices that utilize a de-emphasis scheme. This behaves exactly like pre-emphasis only the signal amplitudes are decreased instead of increased. By decreasing the output amplitude of the driver, it is possible to reduce the effects of crosstalk on these high speed signals.

Clock Distribution

While a lot of attention has been given to the ever-increasing speed of serial data transmission, it is important to understand that system clocks may not be making the same quantum leaps in speed, but that levels of accuracy required for system operation have matched the data-path step for step. With faster and higher-resolution ADC and DAC devices, clock specifications are critical for optimum system performance.

Clock Distribution Topics

- M-LVDS technology and specifications
- Using M-LVDS for clock applications
 - LVPECL comparison
 - ATCA backplane requirements and analysis
- Standard LVDS devices for clock distribution



Before clocks are multiplied, divided, and cleaned, they must be distributed across the system. In the case of larger systems with complex backplane configurations this task ideally handled by devices like the Multipoint Low Voltage Differential Signaling (M-LVDS) family from National.

PCI Industrial Computer Manufacturing Group (PICMG), is a consortium of more than 600 companies who collaboratively develop open specifications for high-performance telecommunications and industrial computing applications.

ATCA, Advanced Telecom Computing Architecture (Advanced TCA®), is the largest specification effort in PICMG's history, with more than 100 companies participating.

Advanced TCA, the PICMG 3.X family, is a new series of PICMG specifications targeted to requirements for the next generation of carrier-grade communications equipment.

The sub-standards within PICMG encompass a large cross-section of high-performance, widely used computing standards in the market now.

PICMG 3.1. Ethernet

PICMG 3.2. InfiniBand

PICMG 3.3 StarFabric

PICMG 3.4 PCI-Express

PICMG 3.5 Rapid IO

PICMG 3.6 PRS (Under Development)

We will use this section of the presentation to compare the ATCA – M-LVDS solution with traditional LVPECL and LVDS clock distribution methods.

M-LVDS

Multipoint, Low-Voltage Differential Signaling

M-LVDS: Multipoint, Low-Voltage Differential Signaling.

This is a key development in National's LVDS technology. These products are specifically tailored to meet the demands of distributed clocking architectures. They have slow, controlled edge rates to reduce system EMI and minimize the transmission line effects of a multi-drop backplane topology.

M-LVDS (TIA/EIA-899)

- **Multipoint-LVDS (described in TIA/EIA-899 standard allows up to 32 driver/receivers**
- **Electrical characteristics include stronger drive, slower edge rate, and wider common mode compared to LVDS (TIA/EIA-644A), all to improve signal quality in a multi-point applications**
- **M-LVDS now specified in ATCA standard for clock distribution, gaining momentum in other areas**
 - *ATCA is the open standard for future modular networks*



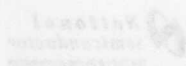
While the original LVDS standard was widely adopted to various and diverse applications, the new TIA/EIA-899 M-LVDS standard is targeted to the very specific needs of multi-point load topologies. This standardization should allow for the widespread adoption of MLVDS into systems that can take advantage of this open multi-source product offering. System designers and architects can look to the M-LVDS family to provide distributed clock solutions for future generations of electronic systems.

Like RS-485, M-LVDS is specified to handle 32 loads. Devices compliant with the M-LVDS standard do not provide as much noise immunity as RS-485, but these devices can provide signaling rates that exceed RS-485 capabilities. In addition to the increased signaling rate, M-LVDS also provides multi-point operation with less power consumption than RS-485.

While TIA/EIA-485 is better suited for longer-distance applications, M-LVDS provides true multi point solutions with less power usage at greater speeds. The lower operating voltages of M-LVDS are the reason for the lower power consumption, but also the reason for the restriction to shorter distances where noise coupling and differential attenuation through the interconnect media are lower.

Family Spec Comparison

	VOD (mV)		Edge Rate (min)	Common Mode	Rx Threshold
	Min	Max			
LVDS	250	450	260 ps	0 to 2.4V	-100 to +100 mV
BLVDS	350	600	260 ps	0 to 2.4V	-100 to +100 mV
M-LVDS DS91D176	480	650	1 ns	-1.4V to 3.8V	-50 to +50 mV
M-LVDS DS91C176	480	650	1 ns	-1.4V to 3.8V	+50 to +150 mV



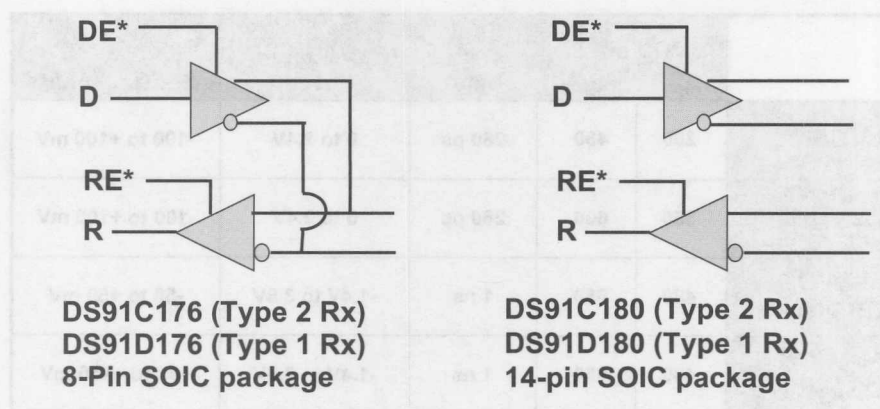
In this chart, some of the key differences between standard LVDS and Multipoint-LVDS are highlighted.

The LVDS devices are designed to drive a point-to-point topology with very low power. This is accomplished with a small voltage swing into a 100Ω termination. Because M-LVDS devices are designed to drive multipoint double-terminated loads, they must provide significantly higher voltage and current to maintain acceptable noise margins in the system.

Another huge difference is the output edge rate. LVDS point-to-point topologies can switch at rates in excess of 1 Gbps. The edge rates need to be sufficiently quick to accommodate this and transmission line losses at higher frequencies. M-LVDS, on the other hand, lives in a low-resistance, high-capacitance environment. This slow edge rate will help eliminate the transmission line effects of stub capacitance.

In addition to the higher VOD, it is important to note that the receiver thresholds have been improved. This reduction improves the signal-to-noise margin in complex multi-drop environments.

no **Device Functionality**



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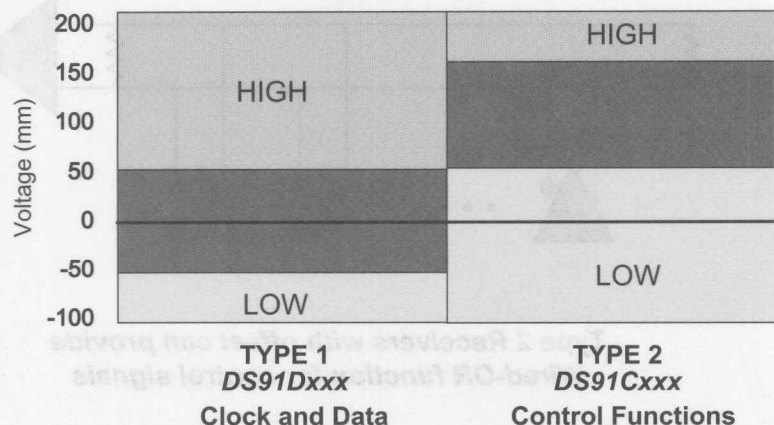
Basic single channel M-LVDS devices – Transceiver – M-LVDS Driver – M-LVDS Receiver:
These are compatible with other vendor M-LVDS offerings.

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Another huge difference is the output edge rate. LVDS point-to-point topologies can switch at rates in excess of 1 Gbps. The edge rates need to be sufficiently quick to accommodate the fast transmission line losses at higher frequencies. M-LVDS, on the other hand, lives in a low-resistance, high-capacitance environment. The slow edge rate will help eliminate the transmission line effects of high capacitance.

In addition to the higher V_{OD}, it is important to note that the receiver thresholds have been improved. This reduction improves the signal-to-noise margin in complex multi-drop environments.

M-LVDS Receiver Thresholds

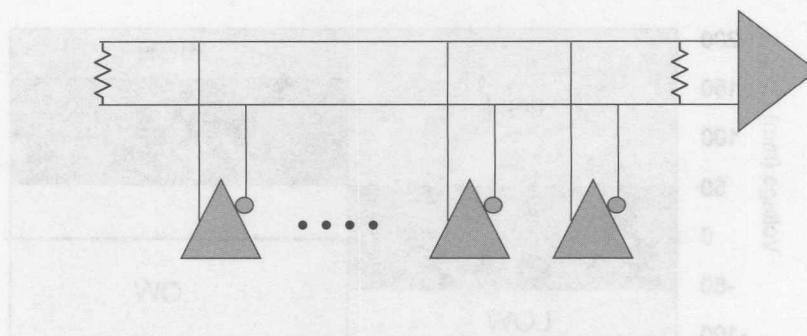


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This graphic highlights the differences between a type 1 and type 2 M-LVDS input. Remember the M-LVDS input thresholds have been tightened by 100 mV; this improves the noise margin in large multi-point designs.

For control functions, the type 2 receiver has been designed to be offset from 0V differential. This allows for a wired-OR control scheme to be implemented with differential signaling. The results are similar to the open-drain style outputs used in LVCMOS control systems.

Type 2 Receiver – Wired OR

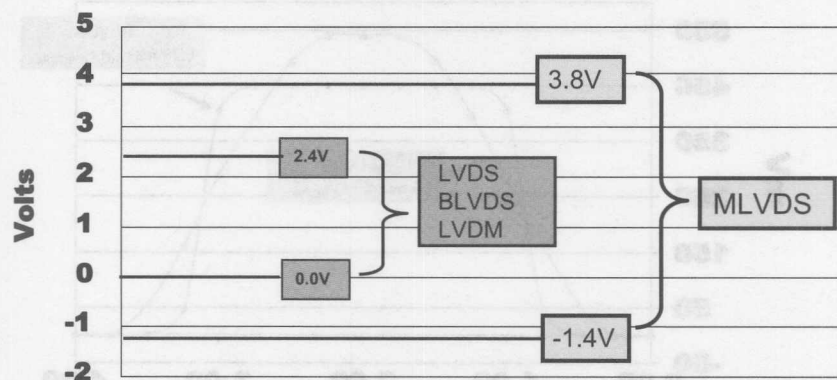


**Type 2 Receivers with offset can provide
Wired-OR function for control signals**



Wired-logic signaling is a common technique used on multi-point bus interface standards. Multiple drivers can pull the control signal high, but when they all go into a Tri-State® condition the type 2 input will respond to the 0V differential with a low output. Examples of standards that incorporate wired-OR logic include the Aontrroller Area Network (CAN), Small-Computer Systems Interface (SCSI), IEEE-488 (GPIB), IEEE-896 (BTL), and others. Often called wired-OR signaling, it provides the equivalent OR gating of all the outputs on the signal line(s) and collision detection. Multi-point protocols most often use wired-logic signaling during bus arbitration, but some also use it during data-transfer phases.

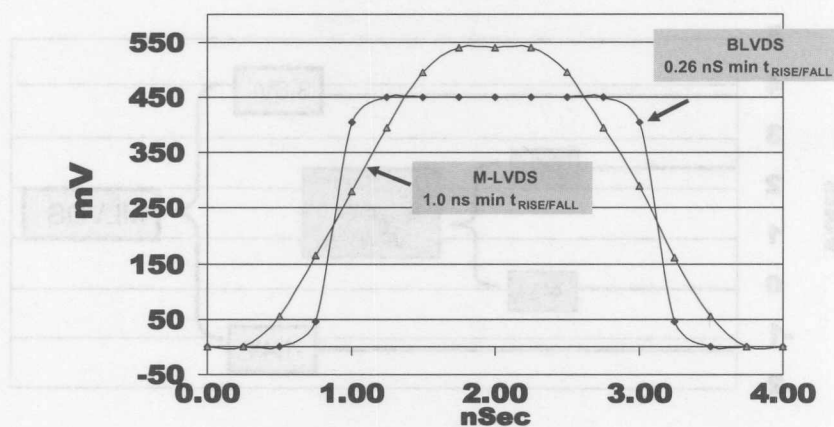
M-LVDS Common Mode Range



The M-LVDS standard includes many unique features to address issues of concern when operating with multi-point communication. The standard allows up to 32 M-LVDS circuits (driver, receiver, or transceiver) to be connected to the common transmission media. The common-mode voltage on a multi-point bus is the sum of the driver output and ground offset voltages. TIA644 and 644-A drivers are required to have an output offset voltage of $1.2V \pm 0.175V$.

Since there are periods when there are no active drivers on a multi-point bus segment, the M-LVDS driver cannot be used to establish the worst-case common-mode operating point of the circuit. During this idle-bus state, the common-mode voltage is bounded by the open-circuit voltages of the attached components. In the case of TIA/EIA-899 compliant devices, this voltage is 0V to 2.4V and is borrowed from its 644 predecessor. The addition of a 1.4V ground-noise offset added to this range gives the common-mode voltage range requirements for M-LVDS circuits of -1.4V to 3.8V.

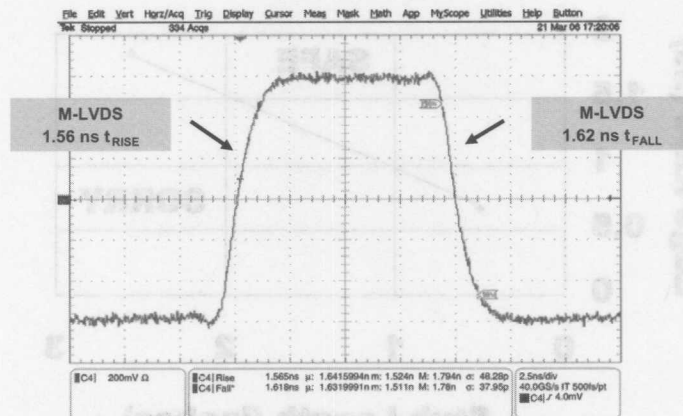
Edge Rate Specifications



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The edge rate of M-LVDS devices is significantly slower than other LVDS families. This significantly improves the signal quality in a multi-point signaling environment.

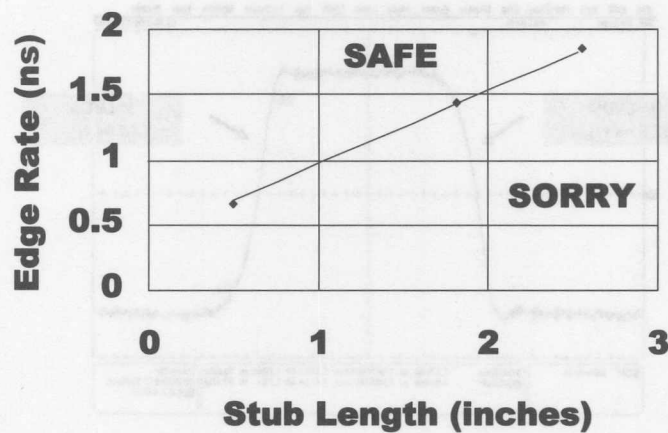
Actual M-LVDS t_{RISE} and t_{FALL}



A final M-LVDS driver provision to address multi-point operation concerns transition time. As was shown in the table on a previous slide, 644 and 644-A allow driver transition times as fast as 260 ps. Faster transition times lead to higher signaling rates, which is one of the key benefits of LVDS.

One of the drawbacks of fast transition times is that careful attention needs to be placed on the design of the interconnect to minimize impedance mismatches from stubs, connectors, and other parasitic connections to the line. General guidelines suggest that mainline stubs be kept as short as possible, with specific guidelines recommending that the propagation delay of a stub be less than 20% of the signal transition time.

Approximate Acceptable Stub Length vs t_{RISE}/t_{FALL}



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For clean backplane waveforms, it is necessary to keep the stubs from acting too much like individual transmission lines. This is achieved by limiting the stub length based on the driver edge rate. Stubs will lower the effective impedance of the backplane traces. Short stubs will still lower the effective impedance, but not significantly impact the signal integrity with reflected energy.

Backplane Clocks

Clock Backplane Application

- LVPECL classically used to drive backplane
 - High-power consumption
- BLVDS has made inroads
 - Good noise margin and much less power than PECL
- Pt-Pt through the backplane still dominates
- “Low” frequency clock distribution (coupled with clock cleaning/multiplication on line card) provides the opportunity for an improved approach
- Multi-point clocking enables:
 - Reduced clock module complexity
 - Reduced backplane etch runs
 - Reduced clock tree power
 - Potential cost savings for customers
- M-LVDS helps by slowing down output transitions improving signal fidelity
- M-LVDS extended common-mode range not required for clock distribution



Traditionally, LVPECL has been used to drive backplane clocks. This type of solution has a relatively high-load current and device power. M-LVDS can be just as effective at distributing low-speed clocks (up to 100 MHz) with a significant savings in power.

M-LVDS vs LVPECL

- I_{CC} vs frequency
 - Single-channel Tx – Rx implementation

	Transmitter	Receiver
M-LVDS	15 mA	10 mA
LVPECL	27 mA	15 mA

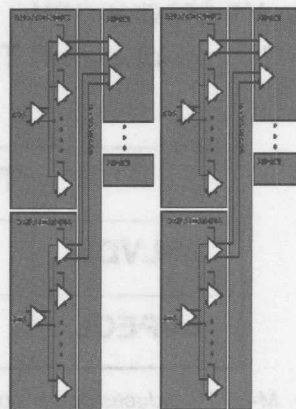
- M-LVDS reduces power consumption by almost 70%



In addition to power, the MLVDS edge rates are slower giving a lower EMI solution.

Backplane Clock Application

- Backplane application
 - Trend to multi-Gbps serial data
 - Usually point-to-point clock distribution
 - Dual clock modules
 - Multiple clock module to line/channel card connections
 - Supply voltage reduction

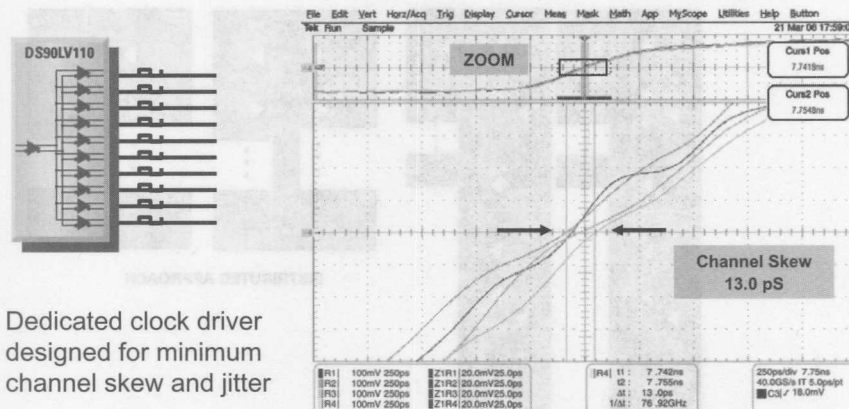


REDUNDANT CENTRALIZED APPROACH



With a redundant centralized clocking approach, each line card will have two independent pairs of incoming clock lines. In a 14-slot backplane, this would mean 28 separate signal pairs to provide clock signals to every line card.

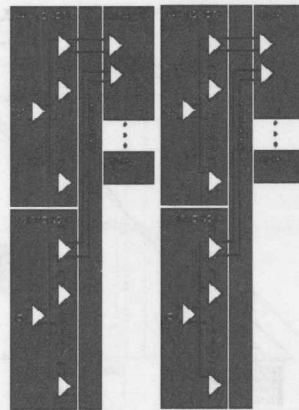
Point-to-Point Clock Design



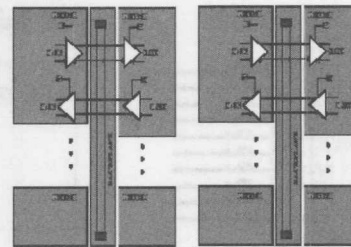
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There are multiple LVDS parts that are ideal candidates for this type of application. In this graphic, the LV110 is shown driving multiple copies of a system clock. Each of the outputs is closely matched to keep channel skew to a very small value. The typical channel skew for LVDS parts in this family are 50 ps or less.

Centralized vs Distributed Clocks



REDUNDANT CENTRALIZED APPROACH



DISTRIBUTED APPROACH

The distributed clocking approach allows for clock distribution with only 10% of the backplane resources. This helps to keep cost of the implementation low. As a side benefit, the clock can be driven from one of multiple sources.

For the central approach, the termination would be provided on each line card. For the distributed approach, the termination is provided at each end of the backplane.

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Standards Work

- **PICMG = PCI Industrial Computer Manufacturers Group**
- **ATCA = Advanced Telecom Computing Architecture**
 - **PICMG** is a consortium of over 600 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications.
 - **ATCA**, Advanced Telecom Computing Architecture (AdvancedTCA®), is the largest specification effort in PICMG's history, with more than 100 companies participating. AdvancedTCA, the PICMG 3.X family, is a new series of PICMG specifications, targeted to requirements for the next generation of carrier grade communications equipment.
 - PICMG 3.1. Ethernet
 - PICMG 3.2. InfiniBand
 - PICMG 3.3 StarFabric
 - PICMG 3.4 PCI-Express
 - PICMG 3.5 Rapid IO
 - PICMG 3.6 PRS (Under Development)



ATCA has incorporated many of today's widely used interface standards and continues to develop additional specifications.

Clock Requirements

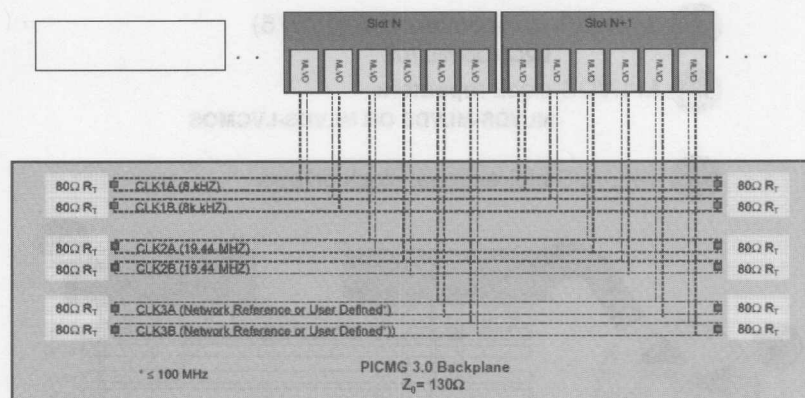
ATCA = PICMG 3.0

- M-LVDS technology shall be used
- Backplane impedance of 130 Ω , terminated with 80 Ω
- Boards interfacing to clock bus must support hot swap
- Clock drivers high impedance unless authorized to drive bus
- Redundant 8 kHz system clock
- Redundant 19.44 MHz SONET/SDH clock
- Redundant third pair of clock signals
 - Network reference signals derived from external inputs
 - User-defined
 - 100 MHz max frequency
 - Reference clock signals can be driven from any slot
 - Source of reference clock is application specific and may change dynamically [Distributed clock architecture]



The M-LVDS technology is central to the clocking scheme of an ATCA backplane. The entire electrical path has been defined to ensure good robust clocking across all possible board permutations.

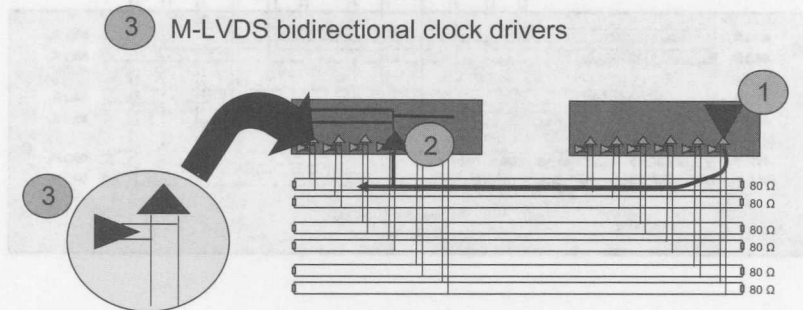
ATCA Clock Bus Architecture



This block diagram details the clock channels. They are all 130Ω differential and doubly terminated with 80Ω at either end of the backplane. The parallel combination of 80Ω resistors means that the M-LVDS devices will be driving a 40Ω -load termination. The maximum stub length from the backplane is defined in the ATCA standard as 1" or 2.5 cm.

ATCA Clock Requirements

- 1 M-LVDS clock drivers (DS91D176)
LVCMOS-MLVDS
- 2 M-LVDS clock repeaters
MLVDS-MLVDS OR MLVDS-LVCMOS
- 3 M-LVDS bidirectional clock drivers



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To support dynamic clock requirements, three types of M-LVDS devices could be used:

Clock driver (LVCMOS to M-LVDS)

Clock repeater (M-LVDS to M-LVDS)

Clock transceiver (Bi-directional LVCMOS / M-LVDS)

ATCA Backplane Performance

M-LVDS devices support 100 MHz operation as required by PICMG 3.0 standard.

Distributed clock architecture is enabled with multi-point LVDS devices.

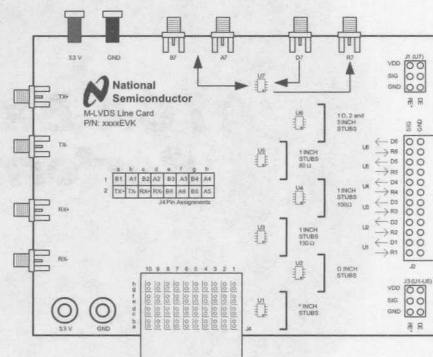
High impedance – hot plug support.

Key signal integrity characteristics:

- 1) Backplane-strength drive capability: Maintains VOD even driving 40Ω load.
- 2) Slow controlled driver edge rates: Keeps stubs at every line card from affecting the signal integrity and noise margin of the distributed clock.
- 3) Provisions for driver contention: For high reliability operation, it is not destructive if multiple drivers contend with each other on the multi-point bus.

M-LVDS Line-card Features

- Compact design: 4 x 3 inches in size
- Six M-LVDS transceivers (DS91D176)
- Stub lengths: 1/4", 1/2", 1", 1 1/2", and 2"
- Stub impedance: 80Ω, 100Ω, and 130Ω
- Two SMA connector pairs connect to I/Os of a single MLVDS transceiver for "device only" evaluation
- Additional two SMA connector pairs for evaluation of the fabric interface with instrumentation and/or available high-speed interface device EVKs (i.e. SCAN15MB200EVK)

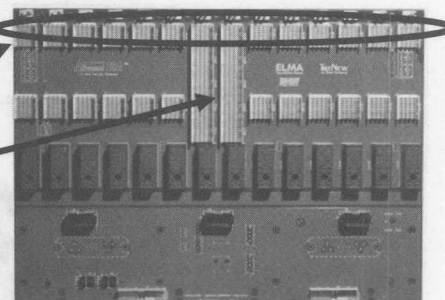


This M-LVDS line card allows for direct plug into ATCA backplane clock. All six clock lines are connected with different stub lengths and impedances to identify optimal line card design. This allows for good observation of clock signals in the real application.

For non-ATCA applications, an additional M-LVDS device is provided with SMA connections on input and output.

ATCA Backplane Features

- Six multi-drop M-LVDS clock pairs
- Dual Star topology for high-speed point-to-point signals
- M-LVDS evaluation line card plugs directly into connectors highlighted in the photo



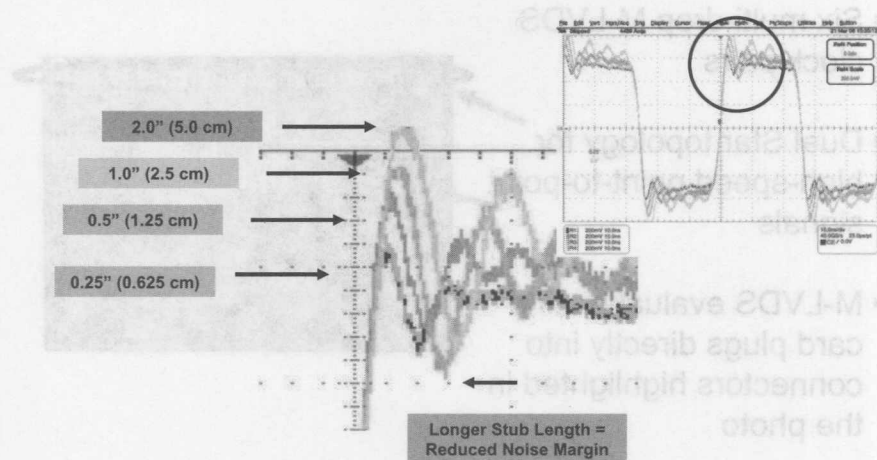
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The six multi-drop clock lines are connected to the backplane headers that are highlighted by the red oval.

The data path is configured in a dual star topology. This means that each fabric or switch card in the center, identified by large connectors, has point-to-point data connections to each line card.

ATCA Stub Length Effects

M-LVDS DS91D176

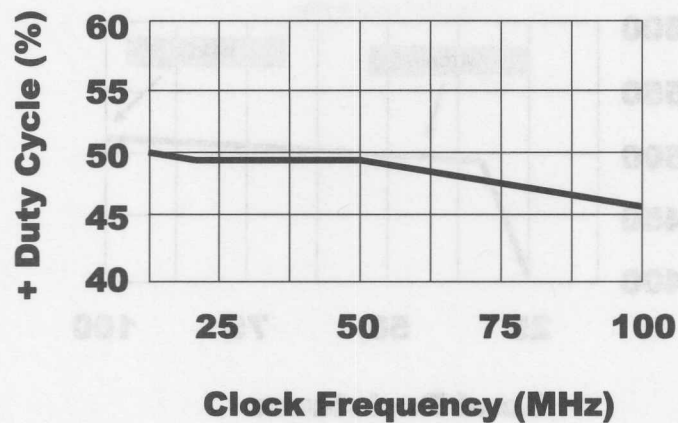


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For clean backplane waveforms, it is necessary to keep the stubs from acting too much like individual transmission lines. This is achieved by limiting the stub length based on the driver edge rate. All the stub lengths will reduce the effective impedance of the backplane clock traces. Short stubs will not significantly impact the signal integrity with reflected energy. Long stubs reduce the overall noise margin available in the design.

ATCA Duty Cycle

M-LVDS DS91D176

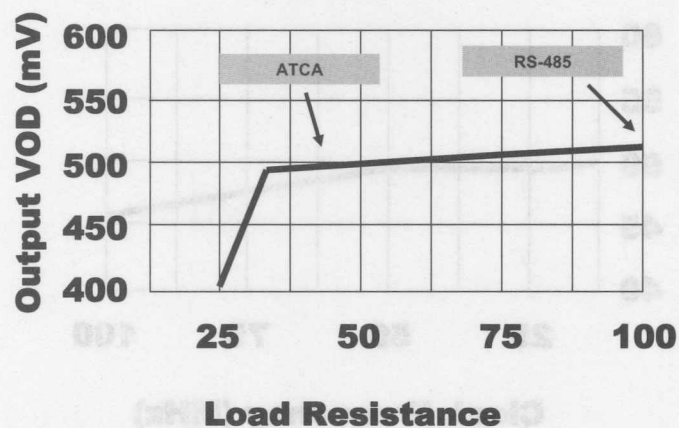


For distributed system clocks, it is critical to maintain a near 50% duty cycle for many components to work properly. The M-LVDS devices have better than 45/55 duty cycle performance all the way to 100 MHz in the ATCA system.

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Output VOD Control

M-LVDS DS91D176

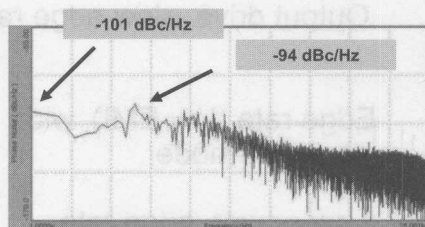


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Even across such diverse loads like the ATCA backplane and RS-485 cabling, the M-LVDS DS91D176 maintains a steady VOD to keep system noise margins high.

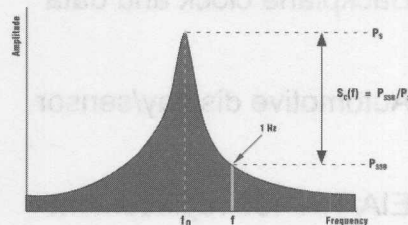
ATCA Jitter and Phase Noise

M-LVDS DS91D176 at 50 MHz



Measurement

- Clock jitter analysis with JIT3 advanced software on TEK6154C (15 GHz Bandwidth)
 - $R_j = 6.5$ ps rms
 - Cycle to cycle jitter = 100 pS_{P-P}



Definition



In most cases, the distributed clock frequency will be multiplied up to some specific frequency and cleaned to ensure the lowest possible phase noise in the signal. This is a phase noise plot of the M-LVDS DS91D176 output.

Phase noise is the measurement of phase fluctuations per unit bandwidth. VCO phase noise is best described in the frequency domain where the spectral density is characterized by measuring the noise sidebands on either side of the output signal center frequency. Single-sideband phase-noise power is specified in decibels relative to the carrier (dBc/Hz) at a given frequency offset from the carrier.

M-LVDS Application Areas

- | | |
|-----------------------------|---------------------------------------|
| • Backplane clock and data | Output drive, slow edge rate |
| • Automotive display/sensor | Edge rate (low EMI), wide common-mode |
| • EIA/TIA-485 replacement | Low-power, edge rate, common-mode |
| • Control signals | Type 2 Rx offset for wired-OR |

Although ATCA is a large early adopter of M-LVDS technology, many other applications are sure to use and benefit from the I/O characteristics of this LVDS family.

Preserving Signal Integrity

Achieving High-Fidelity Signal Amplification

High-voltage (30V), low-noise ($<2.7 \text{ nV}/\sqrt{\text{Hz}}$), operational amplifiers are essential when the primary design criteria is maintaining AC signal fidelity and integrity. We will look at why 30V, low-noise operational amplifiers are superior to lower voltage amplifiers.

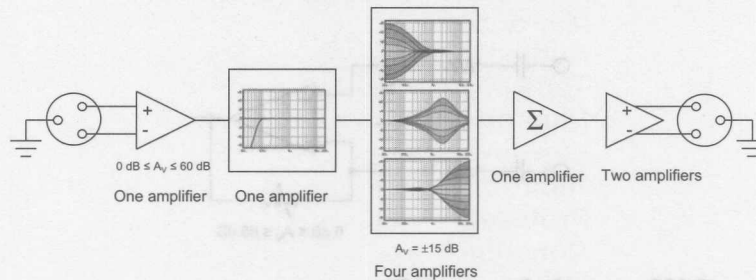
Low Noise Amplification of Low-Level AC Signals

- **Signal sources include:**
 - Microphones
 - Audio DACs (16 bits to 24 bits)
 - Tape head
 - Phonograph cartridges
 - Low-level instrumentation
- **Applications:**
 - Professional audio
 - Consumer audio
 - Industrial instrumentation
 - Sensors
 - Low-level measurement
 - Low-level signal amplification



These low-level signals have a typical amplitude in the range of $0.2 \text{ mV}_{\text{RMS}}$ to $5 \text{ mV}_{\text{RMS}}$. This amplitude needs to be increased to something on the order of $1.5 \text{ V}_{\text{RMS}}$ (with a gain of 77 dB to 50 dB), adding as little additional noise and distortion as possible.

Typical Mixing-Console Signal Path – From μV to V



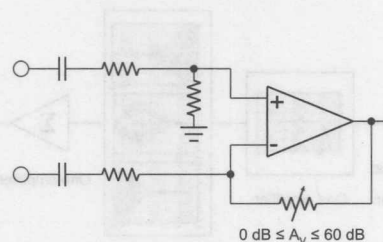
- Signal path can include 9 or more amplifiers
- Noise floor multiplied 3x



From input to output, a typical mixing console may have up to nine amplifiers in the signal path and a total maximum gain of 75 dB. These amplifiers are typically implemented with operational amplifiers. This is the kind of application that demands very low noise and vanishingly low distortion in each individual amplifier to maintain excellent signal integrity and fidelity.

As shown in the figure above, a typical mixing-console signal path is composed of a microphone preamplifier, a high-pass filter, equalization that provides low-, middle-, and high-frequency response adjustments, a summing section for mixing the different signal inputs, and an output amplifier (single-ended and/or differential). It is possible that the entire signal path can use up to 10 amplifiers. The total amplifier noise in the 9-amplifier signal path shown above can be as high as three times the noise of a single amplifier.

Typical Mixing-Console Microphone Preamplifier



- Differential amplifier
- DC blocking capacitor for phantom microphone power



To the microphone preamplifier, a typical ribbon microphone looks like a source impedance of 300Ω . The equivalent voltage noise density for this 300Ω source impedance is $2.22 \text{ nV}/\sqrt{\text{Hz}}$ * or $0.393 \mu\text{V}_{\text{RMS}}$ over a 20 Hz to 20 kHz (noise) bandwidth. This exceedingly small amount of noise is one strong reason for needing low-noise operational amplifiers. The dominant components of the preamplifier's output noise are the microphone's and the amplifier's noise voltage over the bandwidth of interest. Assume the amplifier noise is $1.7 \mu\text{V}_{\text{RMS}}$, for example. Since the noise sources are uncorrelated, the total noise is the square root of the sum of the squares of each noise voltage contribution. The product of the microphone's noise and the amplifier's noise voltage is:

$$\sqrt{(1.7 \mu\text{V})^2 + (0.39 \mu\text{V})^2} = 1.74 \mu\text{V}$$

When using the preamplifier's maximum gain of 60 dB, the noise floor voltage could rise to 1.74 mV. Microphones have a typical dynamic range of 120 dB. This dynamic range results in a maximum output voltage of $1.95 \text{ V}_{\text{RMS}}$. At full output, the microphone preamplifier gain needs to be only 14 dB. At this gain, the noise floor voltage only rises to $24.5 \mu\text{V}$. This is a SNR of 112 dB.

*A resistor has an rms voltage noise density ($\text{nV}/\sqrt{\text{Hz}}$) of

$$V_R = \sqrt{4kTR} = 0.13\sqrt{R}$$

For $T = 298^\circ\text{K}$ and k (Boltzmann's constant) = 1.38×10^{-23}

Differential vs. Single-Ended Inputs



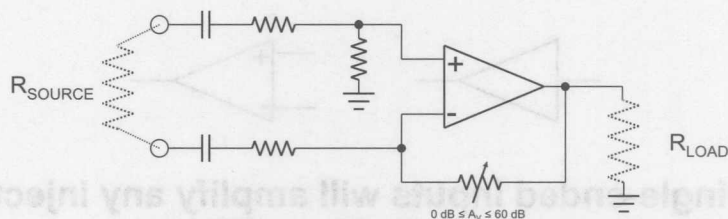
- Single-ended inputs will amplify any injected noise (typically 50/60 Hz or RFI)
- Differential inputs amplify the difference between the two applied signals
- Differential inputs reject noise that is common to the two inputs



Single-ended inputs and outputs are susceptible to noise injection such as AC line frequencies (50/60 Hz and its harmonics). Any signal appearing on the single-ended input will be passed through to the output and amplified if the closed-loop gain is greater than unity.

A differential input can be as susceptible to receiving the same kind of noise as the single-ended input, but if the noise on each input is equal in magnitude and in phase (common-mode noise), it will be rejected by the differential amplifier.

Other Noise Sources



- To ensure lowest noise floor, minimize source resistance
- Noise = $0.13 \text{ nV}/\sqrt{\text{Hz}}$ (at 25°C)
- 600Ω is pro audio standard load and source resistance – but can be even lower
- This load requires high drive current ($\pm 25 \text{ mA}$, minimum) at $\pm 15\text{V}$ output swing

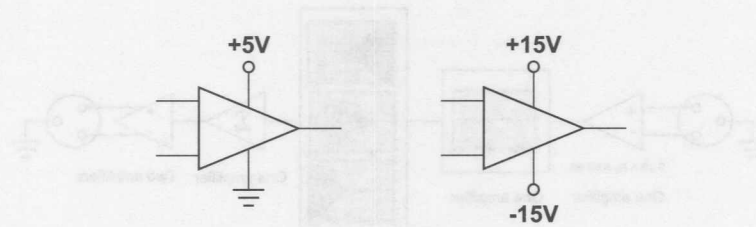
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As was previously mentioned when discussing the typical microphone preamplifier, the source impedance contributes noise to the signal of interest. The nominal magnitude of the Johnson noise in a 1Ω resistor at room temperature is $0.13 \text{ nV}/\sqrt{\text{Hz}}$. The nominal voltage noise density of a 100Ω resistor, a $10 \text{ k}\Omega$ resistor, and a $1 \text{ M}\Omega$ resistor is $1.3 \text{ nV}/\sqrt{\text{Hz}}$, $13 \text{ nV}/\sqrt{\text{Hz}}$, and $130 \text{ nV}/\sqrt{\text{Hz}}$, respectively.

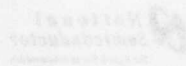
Professional audio applications typically use 600Ω as source and load resistances. The nominal voltage-noise density of a 600Ω resistor is $3.2 \text{ nV}/\sqrt{\text{Hz}}$.

The relatively low 600Ω load requires amplifiers with a minimum output current capability of $\pm 25 \text{ mA}$.

Higher-voltage operation: 5V vs $\pm 15V$



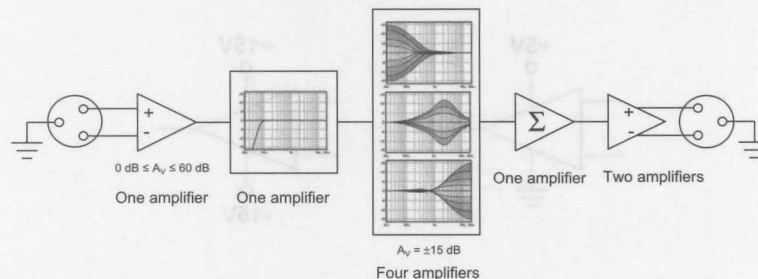
- More swing results in higher SNR
- 5V vs 30V: ≥ 15.6 dB improvement



Modern trends in the semiconductor industry mean that there are a great many low-voltage (5V to 15V) amplifiers available. However, the existence of higher-voltage amplifiers with low noise and distortion will help designers maximize the dynamic range achieved by their designs.

With all else being equal, simply using a $\pm 15V$ supply amplifier instead of a 5V amplifier improves SNR by at least 15 dB.

THD+N



- Multiple amplifiers
- Like noise, want lowest THD+N
- Minimizes increasing THD+N through signal path

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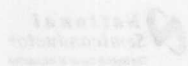
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In a multi-amplifier signal processing chain, low amplifier Total Harmonic Distortion (THD) is necessary to ensure that the overall system linearity and signal integrity is maintained. The amplifier also will add a noise component (N) to the input noise along with the THD. In a measurement system it can be difficult to distinguish between these contributions so the term THD+N is used. The lower THD+N the better because THD+N will increase through the signal chain. Each amplifier adds to the THD+N that all the previous amplifiers in the signal path have contributed. Also THD+N sources are assumed to combine as the square root of the sum of the squares of the individual sources.

THD+N will nominally increase by an order of magnitude for each 20 dB of gain. Therefore, an amplifier with 0.001% unity gain THD+N would measure as 0.1% THD+N at 40 dB of gain.

Slew Rate and Signal Bandwidth

- **Slew Rate (SR):** maximum output voltage rate of change
- **Above some frequency/amplitude combination, slew rate is exceeded**
- **$SR(V/\mu s) = 2\pi \times f_{MAX} \times V_P$**
- **Min slew rate for 20 kHz, 30 V_{P-P} signal: 1.88 V/ μ s**
- **Max frequency for 20 V/ μ s, 30 V_{P-P} signal: 212 kHz**



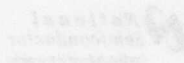
Slew rate is the maximum rate of change that an amplifier's output can sustain and is considered the large signal performance limit of the amplifier. Reaching and exceeding an amplifier's maximum slew rate causes the amplifier to cease operating in a small signal mode, and the output swing no longer accurately represents the input signal. Picture a sine wave morphing into a triangle waveform. Exceeding an amplifier's slew rate is a function of the combination of input signal frequency and magnitude. It is a trade-off: To avoid exceeding an amplifier's slew rate, a high-frequency signal demands lower signal swing, whereas low-frequency signals allow much high signal swing.

In the first of the two examples above, the minimum slew rate needed to amplify a 20 kHz signal that swings ± 15 V_{P-P} is 1.88 V/ μ s. An amplifier with 20 V/ μ s slew rate can amplify a 212 kHz, ± 15 V_{P-P} signal.

Well before the slew rate limit is reached, the amplifier input signal differential voltage is no longer zero (or very small), and distortion will begin to increase. This is why an audio operational amplifier needs a slew rate that is well above the minimum needed for the expected bandwidth and signal swings.

So, What is Needed?

- Low noise
- Low THD+N
- High slew rate
- High power-supply voltage
- High output current



For the example application shown, which shares the same requirements as the vast majority of other high-accuracy, AC signal processing applications, what are the important capabilities needed in an operational amplifier?

Low noise, low THD+N, and high slew rate are essential to ensure signal integrity and fidelity. High power-supply voltage is necessary to maximize signal-to-noise ratio and dynamic range. The low load impedances used to maintain low-noise operation require an amplifier with high output-current capability.

Key Overture® LM4562 Parameters

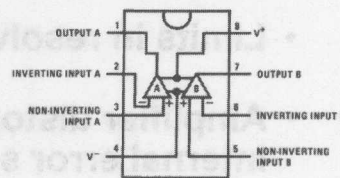
Features

- Low noise: $2.7 \text{ nV}/\sqrt{\text{Hz}}$ ($1.6 \text{ pA}/\sqrt{\text{Hz}}$ at 1 kHz)
- Low distortion: **0.00008%**
- Low I_{BIAS} : 15 nA
- Operating voltage: $\pm 2.5\text{V}$ to $\pm 17\text{V}$
- I_{OUTMAX} : 28 mA
- GBW: 60 MHz
- Slew Rate: 20 V/ μs
- Drives 600Ω
- PSRR and CMRR >110 dB
- Channel-to-channel isolation >130 dB*

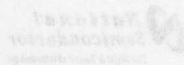
Applications

- Ultra high-quality audio amplification
- High-fidelity preamplifiers
- High-fidelity multimedia
- State-of-the-art phonograph pre amps
- High-performance professional audio
- High-fidelity equalization and crossover networks
- High-performance line drivers
- High-performance line receivers
- High-fidelity active filters

Dual-In-Line Package



*Limited by measurement equipment



The LM4562 is a dual, low-noise, high-voltage, ultra-low distortion operational amplifier designed to meet the requirements of the applications previously shown. It has a typical $2.7 \text{ nV}/\sqrt{\text{Hz}}$ voltage noise density, near perfect linearity with a distortion of only 0.00003% (20 Hz to 20 kHz, $V_{\text{OUT}} = 3 V_{\text{RMS}}$). Its wide $\pm 2.5\text{V}$ to $\pm 17\text{V}$ supply voltage range makes it perfect for professional and high-end consumer audio applications and the perfect upgrade in applications currently using 5V, 12V, and 15V power supply voltages.

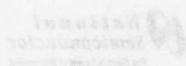
The high 110 dB PSRR and CMRR performance means that external noise, whether coming through the power supply or injected into the LM4562's inputs, will not degrade the amplifier's outstanding performance.

Although it is a dual amplifier in an industry-standard eight-pin package, the 130 dB channel-to-channel isolation ensures that each amplifier will amplify only its intended signal, despite what the adjacent channel it doing.

Finally, the LM4562 is able to easily drive 600Ω loads to within 1.2V of the supply rails.

Measuring THD+N

- Limits in resolving $\text{THD+N} < 0.0005\%$
- Amplifier distortion is an input-referred internal error source
- Increase amplifier's error signal gain
- Closed-loop gain remains unchanged
- Error correcting feedback is reduced

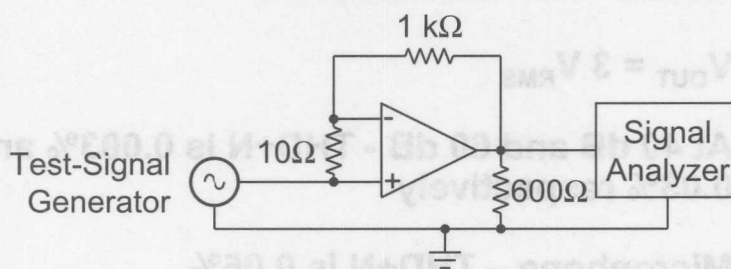


The LM4562 is so linear that it is not possible to directly measure the distortion at unity gain. Even with equipment that can resolve 0.0005% THD+N, the LM4562's actual THD+N is below the test equipment's resolution and is not revealed.

The LM4562's distortion can be considered an input-referred internal error source. To get a closer look at the actual THD+N, amplifying the LM4562's error signal is recommended. The LM4562's closed-loop gain can be left unchanged even while the error signal is amplified. The addition of a single resistor is used to lower the distortion reducing feedback.

THD+N Measurement Circuit

- Signal gain = 1
- Distortion gain = $1 + \frac{1 \text{ k}\Omega}{10\Omega}$ (40 dB)



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In this THD+N measurement circuit, the signal gain is left at unity, whereas the distortion gain has been increased by 40 dB. All that is needed is a 10Ω resistor connected between the inverting and non-inverting inputs.

With the increased amplitude of the distortion components, the measurement equipment is now able to easily revolve the error magnitude. If the measurement value is 0.003%, we know that this is actually 101 (40 dB) times the actual value. How does this translate into an adjusted THD+N value? It is known that when a number's decimal point is moved either left or right by one digit, the number's magnitude changes by a factor 10 (20 dB).

LM4562 THD+N

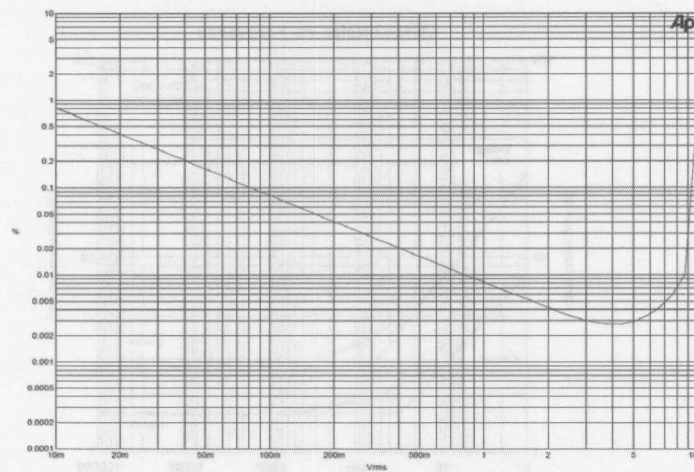
- Measured THD+N is 0.003%
- Input referred with a gain of 40 dB
- Actual THD+N is 0.00003%
- $V_{OUT} = 3 V_{RMS}$
- At 40 dB and 60 dB - THD+N is 0.003% and 0.03% respectively
- Microphone – THD+N is 0.05%



The measured LM4562's THD+N is 40 dB higher than actual. This 40 dB (a 100:1 factor) allows the decimal point to move two digits to the left. Hence, the actual distortion is 0.00003%.

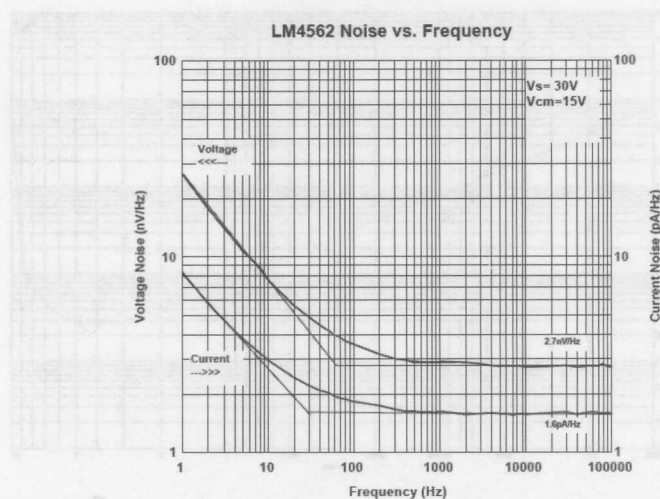
An important reason for using the LM4562 as a microphone preamplifier is its 0.00003% THD+N. When gains on the order of 40 dB to 60 dB are used in an LM4562-based microphone preamplifier, the THD+N is increased to as much as 0.03%. Fortunately, the preamplifier's distortion is still below the typical high-quality microphone which has a THD+N of 0.05%. Therefore, the LM4562's outstanding THD+N performance preserves the integrity and fidelity of a microphone's output signal.

LM4562 THD+N



Here is an actual curve of the LM4562's THD+N versus V_{IN} . This curve was generated with a distortion signal gain of 101 (40 dB). Shifting the decimal point two places to the left to compensate for the gain gives a final THD+N value of 0.00003%.

Voltage and Current Noise Density Curve



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The most important LM4562 feature is a very low voltage-noise density. The typical flat-band voltage noise density is $2.7 \text{ nV}/\sqrt{\text{Hz}}$ with a nominal corner frequency of 60 Hz. The typical flat-band current noise density is $1.6 \text{ pA}/\sqrt{\text{Hz}}$ with a nominal corner frequency of 30 Hz.

How low is this voltage-noise density? The LM4562 has the same nominal voltage-noise density as a 431Ω resistor.

Calculating Voltage Noise for a Given Bandwidth

- Starting with the voltage noise density ($\text{nV}/\sqrt{\text{Hz}}$)
- The noise for a given bandwidth (20 Hz to 20 kHz, for example)
- $\text{Noise}_{\text{BW}} = (\text{nV}/\sqrt{\text{Hz}}) \times (\sqrt{\text{Hz}_{\text{UpperLimit}} - \text{Hz}_{\text{LowerLimit}}})$
- The LM4562 has a $2.7 \text{ nV}/\sqrt{\text{Hz}}$ voltage noise density
- Noise over 20 Hz-to-20 kHz bandwidth:
 $0.48 \mu\text{V}_{\text{RMS}}$
- SNR: 124.2 dB (referenced to $0.775 \text{ V}_{\text{RMS}}$)



The nominal rms noise for any given bandwidth over which an amplifier operates is given by

$$n_{\text{BW}} = (\text{Voltage Noise Density}) \times (\sqrt{\text{Bandwidth}})$$

For the LM4562, operating over a 20 Hz-to-20 kHz bandwidth, the nominal rms noise voltage is

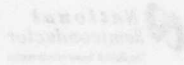
$$n_{\text{BW}} = \frac{2.7 \text{ nV}}{\sqrt{\text{Hz}}} \times \sqrt{(20 \text{ kHz} - 20 \text{ Hz})} \cdot 1.57$$

or $0.48 \mu\text{V}_{\text{RMS}}$

Referenced to the voltage that creates 1 mW dissipation in a 600Ω load ($0.775 \text{ mV}_{\text{RMS}}$), the LM4562 has an SNR of 124.2 dB. Referenced to the LM4562's maximum output when driving a 600Ω load ($+13.8 \text{ V}_{\text{P-P}}$ or $9.76 \text{ V}_{\text{RMS}}$), the LM4562's SNR is 148.2 dB.

LM4562 Audio Operational Amplifier – Preserving Signal Integrity

- Outstanding performance preserves low-level signal integrity and fidelity
- 2.7 nV/ $\sqrt{\text{Hz}}$ voltage noise density
- 0.00003% THD+N ($R_L = 600\Omega$, $V_{\text{OUT}} = 3 V_{\text{RMS}}$)
- 600 Ω load drive
- $\pm 13.8\text{V}$ output swing ($R_L = 600\Omega$, $V_S = \pm 15\text{V}$)

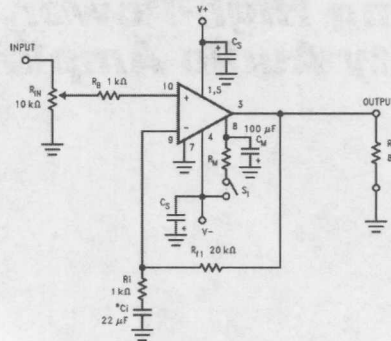


Designing High-Power, High-Fidelity Audio Amplifiers

The challenge in designing a high-performance, high-power amplifier is that high voltage and high output current are required. Furthermore, semiconductor devices are limited to output power levels of 100W or less because of package power dissipation limitations. The LM3886, for example, has an output power of 60W.

Design Challenges

- Requires high voltage and high output current
- Monolithic designs limited to $\leq 100\text{W}$
- E.g. LM3886, monolithic 68W amplifier (see application circuit)

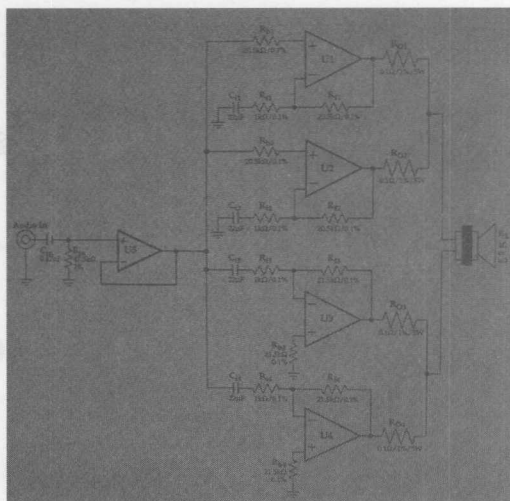


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The challenge in designing a high-performance, high-power amplifier is that high voltage and high output current are required. Furthermore, monolithic designs are limited to output power levels of 100W or less because of package power dissipation limitations. The LM3886, for example, has an output power of 68W.

Increasing Output Power by Using a Different Topology

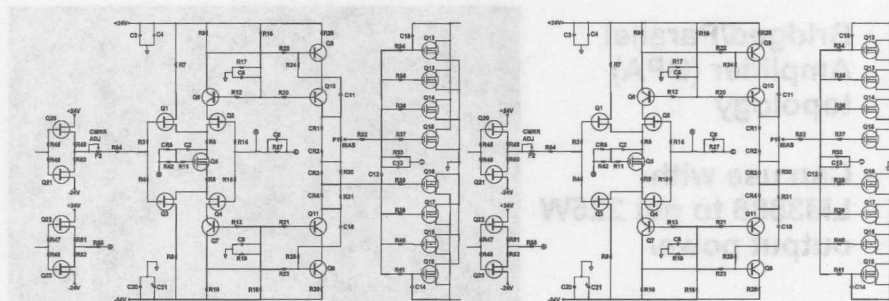
- Bridged/Parallel Amplifier (BPA) topology
- Can use with LM3886 to get 225W output power



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Different amplifier topologies can increase the output power beyond what a single monolithic amplifier can produce. One such topology is the Bridged/Parallel Amplifier (BPA) topology, which can deliver 225W when implemented with several LM3886 amplifiers.

Discrete Designs



• Pro:

- High power
- High fidelity

• Con:

- Size
- Cost
- Complexity
- Design expertise

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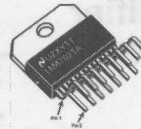
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Another solution is to use a discrete amplifier design. Such a design can use either a MOSFET or bipolar output stage. The pros of this type of design are that high power and high fidelity are attainable. The cons of this approach are the complexity of the design, cost of discrete components, and the need for design expertise.

LM4702 Overture® Stereo High-Fidelity Power Amp Driver

Features

- Very high voltage operation
- Scalable output power
- Minimum external components
- External compensation
- Thermal shutdown and mute



Grades B/C

B – Apps requiring high fidelity & voltage
C – Pro Audio, Industrial, etc

Grade A

Target: Special Applications

Key Specifications

- Three performance grades available: A, B, C
- Wide operating voltage range** C = ± 20 to ± 75
B = ± 20 to ± 100
A = ± 20 to ± 100 **

Grade C Specs

- Output Noise (A-weighted)
- PSRR (input referred)
- THD
- Slew rate

90 μ V
110 dB
0.005%
 ± 15 V/ μ s

** In characterization: Target = 200V (± 100 V)

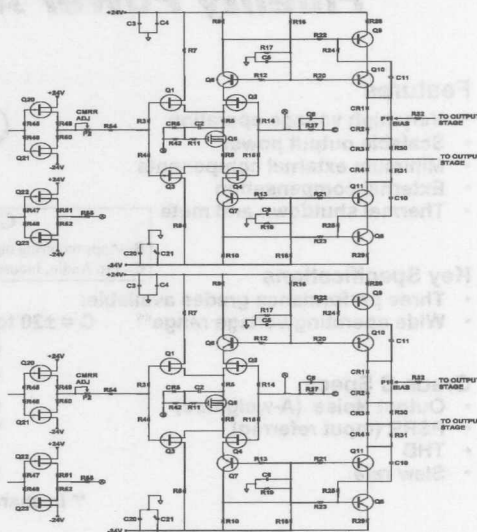


The LM4702 is a high-fidelity audio power amplifier driver designed for demanding consumer and pro-audio applications. When used to drive external power transistors, the LM4702 is capable of delivering in excess of 300W per channel single-ended into an 8 Ω load.

The LM4702 is available in three grades that span a wide range of applications and performance levels. The LM4702C is targeted at high-volume applications. The LM4702B (in development) includes a higher voltage rating along with the tighter specifications. Both the LM4702C and LM4702B come in a TO-220 package. The LM4702A (in development) is the premium part with the highest voltage rating, fully specified with limits over voltage and temperature, and is offered in a military 883 compliant TO-3 gold-plated package.

LM4702 Advantages

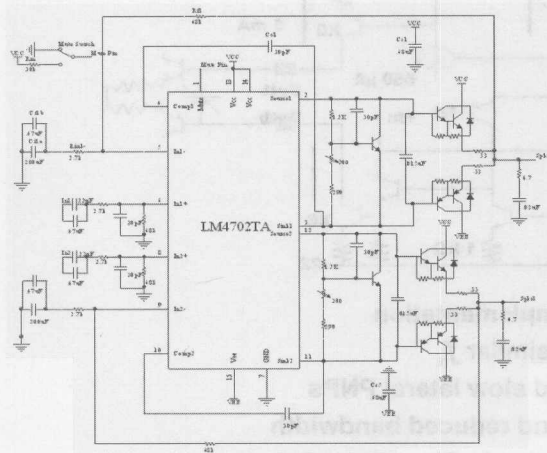
- Replaces entire stereo amplifier front end (see schematic)
- Reduces circuit board space, design time and cost
- No heatsink required



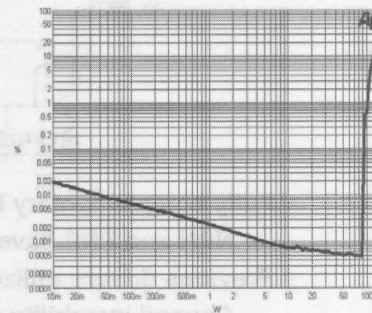
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This is a schematic for the front end of a high-power stereo amplifier. The LM4702 replaces this entire circuit, reducing circuit board space, design time, and cost. The LM4702 itself does not require a heat sink.

LM4702 100W Stereo Demo Amplifier (.0005%THD+N)



THD+N vs P_{OUT} Graph

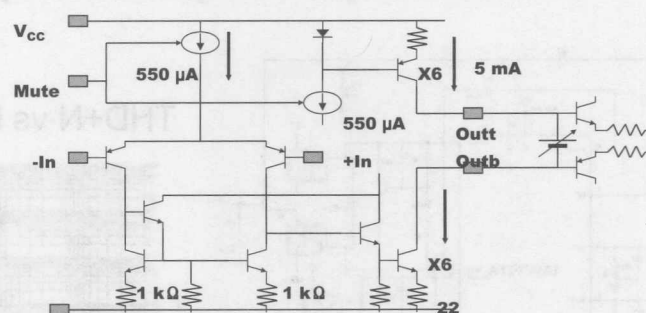


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This is a schematic of a complete 100W stereo amplifier. Notice how few parts are needed for a complete amplifier that uses the LM4702. It uses far fewer components, and as such, is much simpler than the schematic shown on the previous slide! As can be seen from the graph, the THD+N reaches 0.0005%.

In practice, the complete amplifier schematic that is shown in this slide will still need power supplies and some sort of output protection circuitry or fuses. National's Audio Group has heatsink modules (used for the power transistors, not the LM4702) with the 100W complete amplifier board mounted on them available for evaluation.

LM4702 Simplified Schematic

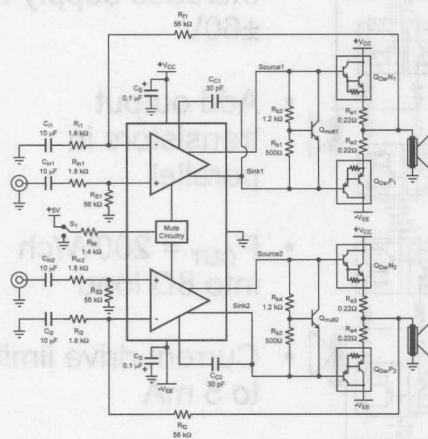


- Fully complementary implementation
 - NPN and PNP have similar f_t
- Previous drivers utilized slow lateral PNPs
 - Caused instability and reduced bandwidth
- Output of LM4702 operates in Class A mode



This is a simplified schematic of the internal circuit of the LM4702. As can be seen from the schematic, it is a fully complementary implementation. In comparison with previous drivers which used slow lateral PNPs, this implementation is superior because the NPN and PNP transistors have similar f_t 's. Another feature is that the output of the LM4702 operates in Class A mode.

LM4702 Output Power Scaling

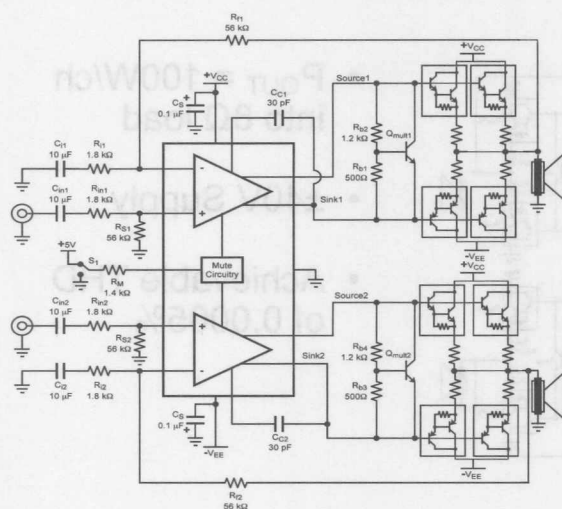


- $P_{OUT} = 100W/ch$ into 8Ω load
- $\pm 40V$ Supply
- Achievable THD of 0.0005%



This is a simplified typical application circuit for the LM4702. With supplies of $\pm 40V$, this amplifier can drive 100W per channel amplifier into an 8Ω load with an achievable THD of 0.0005%. The portion of the circuit enclosed in the rectangular box corresponds to the LM4702. The LM4702 drives an external Class AB output stage, consisting of bias voltage circuitry and power transistors (Darlington's shown). If a designer wanted to increase the output power, how would this be accomplished?

LM4702 Output Power Scaling



- Increase supply to $\pm 60V$
- Add output transistors in parallel
- $P_{OUT} = 200W/ch$ into 8Ω load
- Current drive limited to 5 mA

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Amplifier output power may be scaled by changing the supply voltage and number of output transistors. If a 200W per channel amplifier is desired (see above schematic), the supply voltage must be increased from $\pm 40V$ to $\pm 60V$ in order to get enough voltage swing across the 8Ω load. Furthermore, because of power dissipation limitations of the output transistors, one output transistor must be added in parallel for each existing output transistor – a total of four additional output transistors. As can be seen from the above schematic, there are now two power transistors in parallel per side (top and bottom) in both channels. If a 350W per channel amplifier is desired (not shown), use a $\pm 75V$ supply and three power transistors in parallel per side in both channels.

Power Supply Requirements

Audio power amplifier supplies must:

- Maintain voltage level under load to produce required output power level
- Supply enough current to meet output power demands
- Have acceptable ripple and regulation
- Meet cost targets



Because music and voice programs have a high dynamic, the demands on a power amplifier supply vary greatly. The power supply needs to maintain the voltage such that the power amplifier can produce the desired output power while also supplying large output currents. With the finite PSRR of the audio amplifier, the power supply should also have acceptable ripple.

Power Supply Options

Power supply design choices:

- Linear regulated supply
 - Voltage stays constant
 - Expensive, complex, adds power dissipation
- Switching supply
 - Good regulation
 - More expensive than unregulated, can add switching noise
- Unregulated supply
 - Low cost, acceptable performance for audio power amplifiers
 - Voltage varies significantly

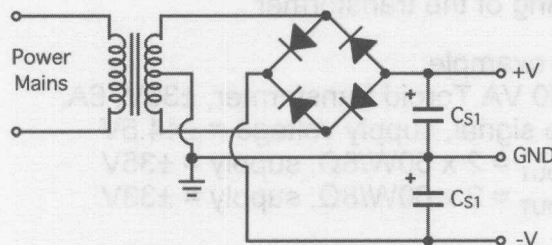
The most common choice is an unregulated supply



A well-designed linear regulated supply will have almost as many components as the audio amplifier portion, and in some cases more. Regulated supplies are more expensive, have higher part counts and reduced reliability, but the voltage is pretty constant. A switching supply has very good regulation, but is still more expensive than an unregulated supply and the switching noise is not something audio designers want in the system. An unregulated supply uses very few parts, is simple, and lower cost with high reliability, but has the drawback that the supply voltage varies much more. The most common choice for customers is to use an unregulated supply.

Unregulated Supply Schematic

- Unregulated supply components:
 - Transformer
 - Diode bridge
 - Supply capacitors



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An unregulated supply is very simple and consist of only a few parts. The heart of the supply, and typically the largest cost, is the transformer. The transformer may be a standard type or a more expensive, but higher performance toroid. The diode bridge can be discrete diodes or a complete bridge in a single package. The supply capacitors are typically designed to act as current reservoirs to stabilize the voltage under high current demands and limit ripple. The current reservoirs consist of large, electrolytic capacitors of value from 470 μF to 20,000 μF or several capacitors in parallel for even higher values. Additionally, there will be another group of capacitors located near the IC(s). Capacitors by each IC for high-frequency noise rejection are typically ceramic chip type in value from 0.01 μF to 0.47 μF and smaller value electrolytic or tantalum capacitor of value from 1 μF to 47 μF used by each IC, as needed.

Unregulated Supply Issues

Supply voltage varies with:

- Output power
- High line condition on mains (or brown out)
- Rating of transformer used in the design
- Heating of the transformer
- Real example:
 - 360 VA Toroid transformer, $\pm 30V$, 6A.
 - No signal, supply voltage = $\pm 44.5V$
 - $P_{OUT} = 2 \times 50W/8\Omega$, supply = $\pm 35V$
 - $P_{OUT} = 2 \times 60W/8\Omega$, supply = $\pm 33V$



Unregulated supplies have a significant amount of voltage variations. The voltage will drop as output current increases. This is called supply droop. A high line condition on the mains will raise the voltage so the maximum rating of the power supply must take this possible condition into account. The rating of the transformer also will affect how much voltage variation occurs. As the transformer heats up, the resistance of the windings will increase, resulting in additional voltage drop. When there is no signal, the supply voltage will float to a higher level since only minimal current is being drawn. The example gives some actual numbers from a design. Notice that the no signal supply voltage rises as high as $\pm 44.5V$, while under a full load the supply has dropped to $\pm 33V$.

Unregulated Supply Issues

- Must allow full output power
- The high-line, no-input-signal supply voltage must not exceed the maximum voltage of the IC
- Large supply capacitors reduce ripple but slow supply droop increasing P_D in the IC. Too much capacitance increases load on and heating of the transformer
- High line condition may increase maximum voltage by 10% more
- Typical regulation ranges from 25 to 50%



As shown in the real example in the last slide, the minimum voltage under full-load conditions results in an unregulated supply that will float up 30% under a no signal condition. If the no signal voltage is lowered, then the full-load voltage also will decrease and the target output power specification would no longer be met. Adding additional capacitance on the supply will help reduce the supply droop, but also slows the rate of supply collapse so that power dissipation is higher in the amplifier IC. High supply capacitance also will increase the current load from the transformer, increasing the heating of the transformer. The result, in order to use an unregulated supply, amplifier ICs must have significant supply head room above the operating supply. This poses a challenge, since the supply is limited by the fabrication process and by design.

Summary

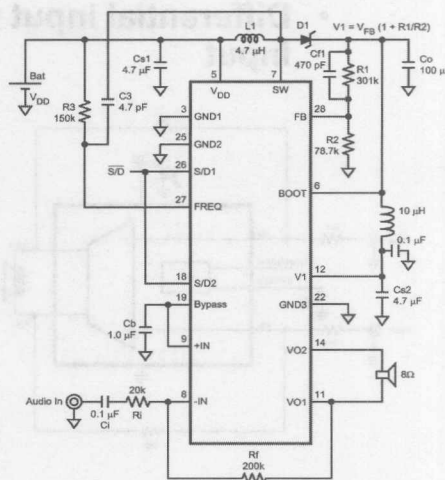
- Use unregulated supplies
- Need adequate headroom above full power supply rating
- Traditional IC supply ranges limited to 100 to 120V
- LM4702 dramatically raises supply voltage to 200V



In summary, unregulated supplies should be used because they are less expensive and give acceptable performance for audio power amplifiers. However, adequate headroom must exist between the nominal power supply voltage and the maximum supply voltage of the IC in order to account for extreme conditions (high line, no input signal). Traditionally, IC supply voltages have been limited to 100 to 120V. The LM4702 is a dramatic improvement with its 200V supply voltage.

More Power-Less Volts

- **LM4804 mono 1.8W BTL amplifier**
- **Operating supply range of 3V to 4.2V**
- **Output power exceeds 2W (THD+N = 10%) over power supply range of 2.9V to 4.2V**

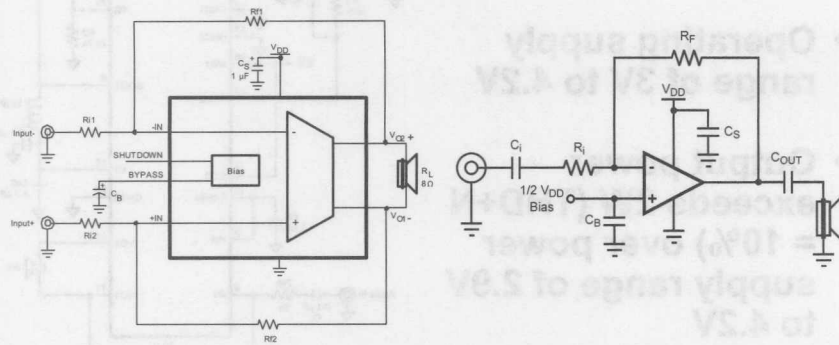


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When relatively low-voltage power supply sources are used, it is more difficult to get high speaker power levels, even with BTL amplifiers. Lower impedance speakers will increase power levels, but at the cost of increased current levels in the amplifier and in circuit traces. A more preferable approach may be to use a boosted Boomer® amplifier, represented here by the LM4804. This amplifier delivers 1.8W to an 8Ω BTL speaker while operating on a battery voltage of just 4.2V. In addition, it will deliver a minimum of 2W (10% THD+N) to that same 8Ω BTL speaker over a battery voltage range of 2.9V to 4.2V.

Maintaining Signal Integrity

- Differential input versus single-ended input



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Low-voltage power amplifiers in portable applications are often subject to interfering signals from adjacent digital and RF circuits. Differential input amplifiers are considered excellent low noise and high PSRR amplifiers when compared to similar single-ended amplifiers. But care must be taken with both to maintain signal integrity on both sides of the amplifier's input. Typically, differential inputs will provide better SNR than single-ended inputs, but this is only true as far as the differential amplifier is designed and laid out properly to maintain balance between the amplifier "halves." Close matching of external components is required to maintain the excellent PSRR and CMRR benefits differential amps provide.

LM4927 Mono, Fully Differential Amplifier

Key Specs

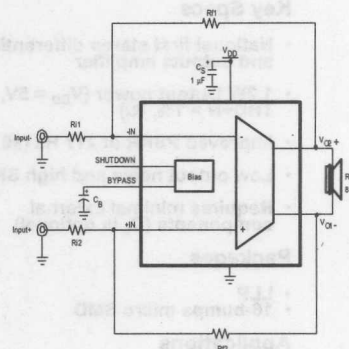
- Differential inputs and outputs
- 1.3W Output power ($V_{DD} = 5V$, THD+N = 1%, 8 Ω)
- Improved PSRR at 217 Hz (87 dB)
- Low output noise and high SNR
- Requires minimal external components (C_B is optional)

Packages

- LLP

Applications

- Mobile phone
- PDA
- Portable electronic devices



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The LM4927 is a mono, fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications.

It is capable of delivering 1.3W watts of continuous average power to an 8 Ω load with less than 1% THD+N from a 5V DC power supply. It has improved PSRR and very low output noise. It also drives 4 Ω loads with 2.1W of output power with 5V DC power supply and less than 1% THD.

LM4928 Stereo, Fully Differential Amplifier

Key Specs

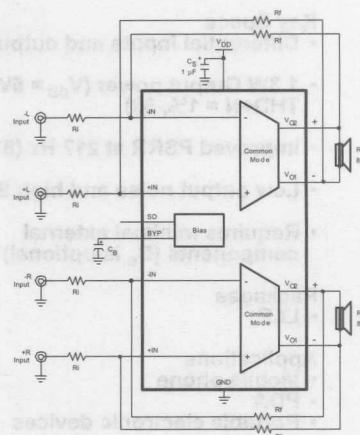
- National first stereo differential inputs and outputs amplifier
- 1.2W Output power ($V_{DD} = 5V$, THD+N = 1%, 8 Ω)
- Improved PSRR at 217 Hz (90 dB)
- Low output noise and high SNR
- Requires minimal external components (C_B is optional)

Packages

- LLP
- 16-bumps micro SMD

Applications

- Mobile phone
- PDA
- Portable electronic devices



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The LM4928 is a stereo, fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications.

It is capable of delivering 1.2W per channel of continuous average power to an 8 Ω load with less than 1% THD+N from a 5V DC power supply. It has improved PSRR and very low output noise.

When supplied in the LLP[®] package it can also drive 4 Ω loads. Output power = 1.8W per channel (4 Ω , THD+N = 1%).

Class D Advantages

- **Efficiency**
 - Longer battery life
 - Important for portable devices
 - Laptops
 - Cell phones
 - Lower device temperature
 - LCD TVs
 - Panel thermal distortion
 - No heatsinking
 - Smaller solution

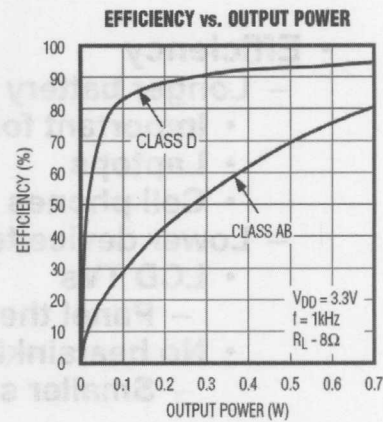
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Class D's main advantage versus Class AB is higher efficiency. This extends battery life, which is critical for portable devices such as laptops and cell phones. Also, the Class D amplifier operates at a lower device temperature for the same rated output power compared to an AB amplifier. This is critical in LCD displays, where heat dissipation from an audio amplifier can cause thermal distortion on the LCD panel itself. Since the Class D amplifier runs at a lower temperature, smaller size heatsinks or no heatsinking at all can be achieved.

Efficiency

- How the Class D is efficient
 - Output MOSFETs operating in the linear region (low resistance switches)
 - Output stage requires no bias current
- Good Class D amplifiers can achieve $\eta > 85\%$



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Here is an efficiency comparison for a typical Class D amplifier versus a Class AB amplifier. Peak efficiency is achieved at a faster rate for Class D. The reason for this is that the Class D's output MOSFETs operate like very low resistance switches, that are either fully on or fully off. Also, the output stage for the Class D does not require any bias current.

Efficiency Losses

- Where it loses power
 - Internal sources
 - $R_{\text{DS(on)}}$
 - Determined by MOSFET size
 - Biggest contributor to efficiency loss
 - Switching losses
 - Time spent in active region
 - Higher frequency, more time in active region
 - Gate current
 - Larger MOSFETs require more gate current
 - Designer must create a balance between switching frequency for best THD+N and efficiency, and MOSFET size and minimum gate current

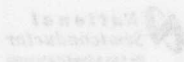
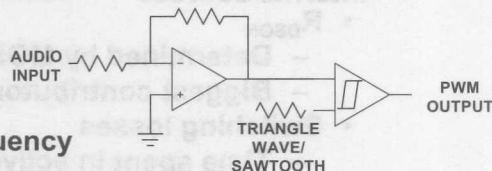


Theoretically, Class D can achieve an efficiency of 100%. Unfortunately, all MOSFETs have a non-zero $R_{\text{DS(on)}}$. The power loss due to $R_{\text{DS(on)}}$ is conduction loss. A voltage divider is formed by $R_{\text{DS(on)}}$ and the output load, which prevents Class D amplifiers from ever reaching their theoretical efficiency. $R_{\text{DS(on)}}$ can be minimized by increasing the MOSFET size. The Class D's gate charge and switching currents also dissipate power, which is considered switching loss. During switching times, losses occur because the rise and fall times of the FETs are greater than zero, since the output transistors cannot switch instantaneously. The more time the output FETs remain in the transition region, the more power is consumed. Also, gate capacitance of the FETs increase rise and fall times, but as MOSFETs become larger, gate capacitance becomes larger as well. To ensure fast rise/fall times of the MOSFETs, the gate driver must provide more gate current to charge and discharge the gate capacitance during the switching interval. Gate currents also contribute to switching losses as well.

PWM Architecture

- **Simplified PWM modulator**

- Sawtooth or triangle waveform used to modulate audio input
- THD+N improves as switching frequency increases
- Higher switching frequency leads to decrease in efficiency
- **Noise (EMI)**
 - PWM at a constant frequency



The majority of Class D amplifiers use a PWM (pulse-width modulated) approach. Here is a simplified view of a PWM modulator. A comparator compares the level of the audio input to a triangle wave operating at a switching frequency significantly above the audio band. Better THD+N performance can be achieved with higher switching frequency. However, EMI can be an issue if the switching frequency is too high. Since traditional Class D amplifiers use a constant switching frequency, the harmonics of that frequency can radiate, which will make EMI emissions worse. The resulting PWM comparator output waveform is then used to drive the H-bridge output stage.

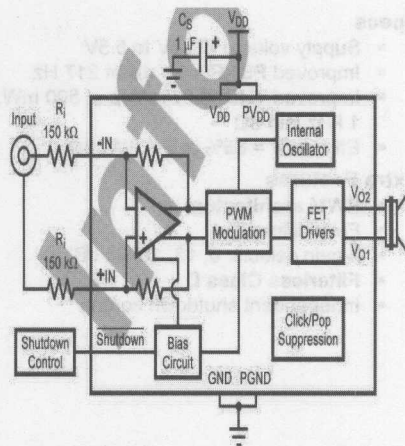
LM4673 Boomer 2.65W Class D Amplifier

Specs

- Supply voltage = 2.4V to 5.5V
- Improved $I_{DDQ} = 2.6 \text{ mA}$ (3.75 mA max) at 5V
- Improved **PSRR = 78 dB** at 217 Hz
- Improved **THD+N: 0.02%** at 3.6V, 100 mW, 1 kHz into 8Ω
- SNR = 97 dB** at 5V, 1W
- Output noise = 23 μA** at 3.6V, A-weighted
- Efficiency = 88%** at 3.6V, 400 mW, 8Ω

Extra Features

- PWM architecture**
- Fully differential
- Filterless Class D** when speakers are close to outputs
- Output short circuit protection



Class D Amplifiers



The LM4673 is a mono PWM class D amplifier with an efficiency rating of 88% for mobile phones, PDAs, and other portable electronics where battery life is important. This is the world's smallest Class D audio amplifier in the 4mm pitch micro SMD package.

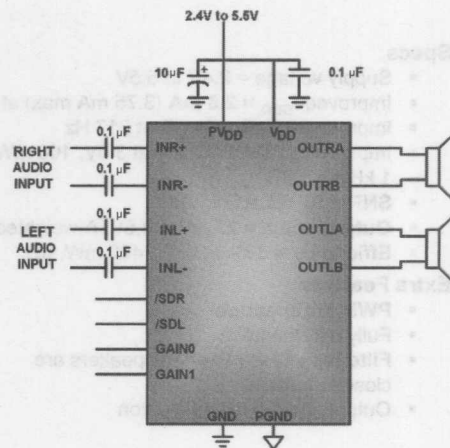
LM4674 Boomer® - Stereo 2.5W per Channel Class D Amplifier

Specs

- Supply voltage = 2.4V to 5.5V
- Improved **PSRR = 74 dB** at 217 Hz
- Improved **THD: 0.07% Typ** at 500 mW, 1 kHz into 8Ω
- Efficiency = **85%** at 5V, 1W, 8Ω

Extra Features

- **PWM architecture**
- Fully differential
- 4 gain selects: 6, 12, 18, 24 dB
- **Filterless Class D**
- Independent shutdown control



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The LM4674 is a stereo version of the LM4673 aimed at multimedia phones and PDAs with stereo speakers.

Analog Video Solutions

Video Standards, Formats, Interfaces, and Signals

The top box contains the analog broadcast TV standards used worldwide. The middle box contains the Electronic Industries Alliance (EIA) specifications for YPrPb analog component video. These EIA 744X specs do not address YCbCr digital component video.

- EIA 744.1 is the U.S. specification for standard component video which includes subcarrier signaling (1.58 MHz) and NTSC systems.
- EIA 744.2 is the U.S. specification for standard-definition TV (SDTV) analog component video which includes 480i and 480p video formats.
- EIA 744.3 is the U.S. specification for high-definition TV (HDTV) analog component video which includes 1080i and 1080p formats.

The bottom box contains the Society of Motion Picture Engineers (SMPTE) specifications for various video signals, including composite (analog signal only), component and RGB video (analog and/or digital signals).

Video Groups and Specifications

NTSC: National Television System Committee. The US form of standard definition TV.
PAL: Phase Alternating Line. The system of standard definition TV implemented in Europe, etc.
SECAM: Sequential Couleur avec Memoire. The French form of standard definition TV.
ATSC: Advanced Television Systems Committee. The US form of high definition TV (HDTV).
VESA: Video Electronics Standards Association. Proposes, publishes video standards for Graphics.
ITU: International Telecommunication Union. Proposes/publishes video standards for EU broadcast.
SMPTE: Society of Motion Picture & TV Engineers. Proposes, publishes standards for US broadcast.
MPEG: Motion Picture Experts Group. Proposes and publishes video standards for Broadcast.
EIA 770.1: The US spec for Enhanced Component video, similar to ITU-R BT1197/ETSI 300 294.
EIA 770.2: The US spec for Standard Definition TV (SDTV) Baseband Component Video.
EIA 770.3: The US spec for High Definition TV (HDTV) Baseband Video.
ITU-R BT.470: Harmonized spec for SDTV world wide, including NTSC, PAL, and SECAM.
ITU-R BT.601: Universal Sampling spec for SDTV / HDTV Broadcast Video. Similar to SMPTE125M.
ITU-R BT1197/ETSI 300 294: Spec for PAL Plus Enhanced TV in Europe.
SMPTE 125M: Similar to ITU-R BT.601.
SMPTE 170M: Has replaced EIA RS 170A, color spec for NTSC.
SMPTE 253M: RGB Analog Video Interface spec for SDTV Studio applications.
SMPTE 274M: Spec for 1920 x 1080 HDTV.
SMPTE 296M: Spec for 1280 x 720 RGB and YPbPr Baseband Video. Similar to PAL Plus.



The top box consists of the analog broadcast TV standards used worldwide.

The middle box consists of the Electronic Industries Alliance (EIA) specifications for $Y_{P_B}P_R$ analog component video. These EIA 770.X specs do not address $Y_{C_B}C_R$ digital component video.

- EIA 770.1 is the U.S. specification for enhanced component video, which includes widescreen signaling (16:9 aspect ratio) for NTSC systems.
- EIA 770.2 is the U.S. specification for Standard-Definition TV (SDTV) analog component video, which includes 480i and 480p video formats.
- EIA 770.3 is the U.S. specification for High-Definition TV (HDTV) analog component video, which includes 720p and 1080i formats.

The bottom box contains the Society of Motion Picture Television Engineers (SMPTE) specifications for various video signals, including composite (analog signal only), component and RGB video (analog and/or digital signals).

Standard-Definition (SDTV) Formats and Timing

NTSC/480i (Interlaced)

- 720 (H) x **480** (V) active video resolution (720 x 240 active/field)
- 858 x **525** total resolution
- V refresh rate (frame rate): 29.97 Hz (59.94 Hz field rate)
- H scan line rate: 15.734 kHz

PAL/576i (Interlaced)

- 720 x **576** active video resolution (720 x 288 active/field)
- 864 x **625** total resolution
- V refresh rate (frame rate): 25 Hz (50 Hz field rate)
- H scan line rate: 15.625 kHz
- A lot of variations (PAL I, B, G, H, D, N, M)



In the United States, older conventional televisions were made for displaying NTSC video, which has an active video resolution of 720 x 480 at 29.97 frames per second or 59.94 fields per second. In other parts of the world, like Europe, PAL video has an active video resolution of 720 x 576 at 25 frames per seconds or 50 fields per second, and is interlaced as well. In interlaced scan systems, two fields (referred to as odd and even fields) are required to scan one picture frame.

Using the PAL format as an example, the odd field, which consists of lines #1 to 312.5, are scanned first. Then, the even field consisting of lines 312.5 to 525 are scanned next. The odd and even fields are scanned at 50 fields/sec, which equates to 25 frames/sec.

The “active video resolution” is considered to be the portion of the visible picture frame on a correctly adjusted display. The “total resolution” includes the active video portion plus “non-active” video portion dedicated to horizontal/vertical sync and blanking, and in the case of composite video, also color burst information.

Most people often refer to video formats by the active vertical resolution per frame plus the scan type, “I” for interlaced and “p” for progressive scan. 480i actually has 525 total lines of vertical resolution (active lines and blanking lines) and has the same timing as NTSC. However, 480i is transmitted via the analog component interface rather than composite interface. 576i has 625 total lines of vertical resolution and has the same video timing as PAL. 576i is like 480i in that it is transmitted via analog component interface.

Enhanced Definition (EDTV) Formats and Timing

480p (Progressive)

- 720 x 480 active video resolution
- 858 x 525 total resolution
- V refresh rate: 59.94 Hz
- H scan line rate: 31.469 kHz

576p (Progressive)

- 720 x **576** active video resolution
- 864 x **625** total resolution
- V refresh rate: 50 Hz
- H scan line rate: 31.25 kHz



Although the EIA 770.2 specification refers to both 480i and 480p as SDTV, 480p is more commonly referred to as Enhanced Definition TV (EDTV) to distinguish it from its less superior, interlaced counterpart. In progressive formats, all the scan lines are scanned in one field/frame, which yields a higher vertical resolution picture per field and reduces visibility of scan lines and flicker. Therefore, 480p and 576p have the same total resolution as 480i and 576i; however, the scan rate is twice as fast, resulting in better picture quality and less viewer fatigue. Progressive scanning is also used in computer monitor displays, but typically at higher resolutions and frame/refresh rates. This results in better looking static images, such as text and graphics.

High-Definition (HDTV) Formats and Timing

720p (Progressive)

- 1280 x **720** active video resolution, “widescreen format” 16:9 (H:V) aspect ratio
- 1650 x **750** total resolution
- V refresh rate: 59.94 Hz
- H scan line rate: 44.955 kHz
- **Tri-level sync**

1080i at 59.94 Hz* (Interlaced)

- 1920 x **1080** active video resolution (1920 x 540 active/field), 16:9 aspect ratio
- 2200 x **1125** total resolution
- V refresh rate (frame rate): 59.94 Hz (29.97 Hz field rate)
- H scan line rate: 33.716 kHz
- **Tri-level sync**

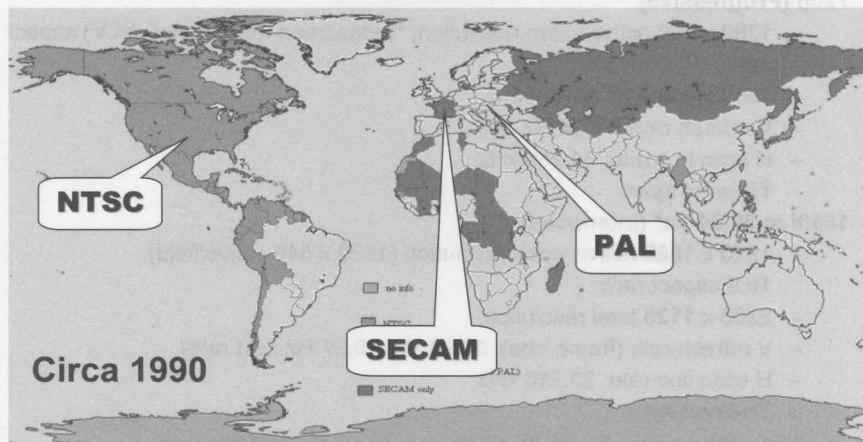
*Other refresh rates like 24, 25, 30 Hz, etc. See SMPTE 274M specs.



The U.S. specification for HDTV includes two major HDTV formats: 720p is progressive and 1080i is interlaced. These formats have much higher resolution than SDTV and EDTV and come close to some computer display resolutions. Both 720p and 1080i have a 16:9 aspect ratio, which is the ratio of active horizontal-to-vertical resolution, which closely resembles the widescreen format of cinema. Standard TV formats are closer to a 4:3 aspect ratio.

Another difference between HDTV signals are the handling of its synchronization, or sync signals, which defines the video format's timing parameters. HDTV signaling uses “tri-level sync,” as opposed to “bi-level” or standard sync found in SD/EDTV signaling. Tri-level sync has faster rise times because of the increased video timing and high bandwidth of HD, which results in more accurate timing edges and better jitter performance. These factors are important to meet the stringent requirements necessary for HDTV sync separation, as we will see later.

Analog Broadcast TV Standards Worldwide



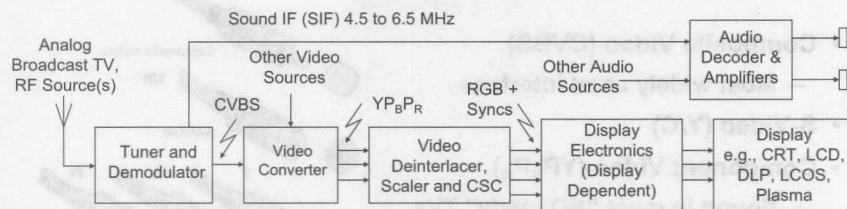
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NTSC is mainly used in the Americas, Japan, and South Korea.

PAL spans many countries in Europe, Asia, and Africa.

SECAM was developed by French engineers, and is used primarily in France, the Middle East, Russia, and Africa.

Example: "HD Ready" TV Set



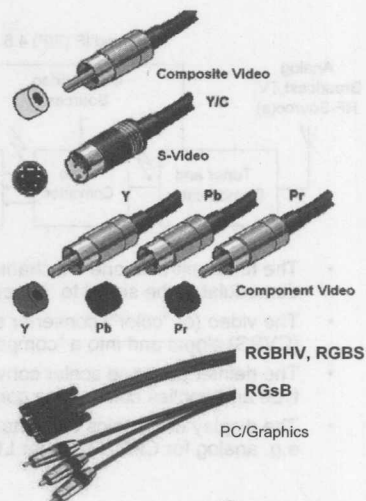
- The tuner extracts one TV channel at a time from many, then downconverts and demodulates the signal to "baseband"
- The video (or "color") converter separates the colors from the "composite video" (CVBS) signal and into a "component video" (YP_BP_R or YC_BC_R) signal
- The deinterlacer and scalar converts the video format to match it to the display type and applies color space conversion (CSC) from YP_BP_R to RGB.
- The display electronics converts the RGB signal to match that of the display type, e.g. analog for CRT, LVDS for LCD panel



This block diagram demonstrates the various levels of baseband video after the tuner/demodulator stage. Several stages of video conversion or decoding are necessary before the video can actually be displayed on-screen. This is a generic example and can vary between display types, such as CRT, LCD, etc.

Analog Video Interfaces

- **Composite Video (CVBS)**
 - Most widely used interface
- **S-Video (Y/C)**
- **Component Video (Y_PB_PR_P)**
 - Found in most “HD ready” TVs
- **PC/Graphics (RGB)**
 - RGBHV – 5-channels
 - RGBS – 4-ch
 - RGsB – 3-ch



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Composite, S-video, and component are the most popular video interfaces for consumer video equipment.

RGB is mostly used for PC/graphic interfaces and comes in three variations, each of which handles sync signals differently. Above, the signals underlined are the ones that carry the sync information.

CVBS: Composite Video

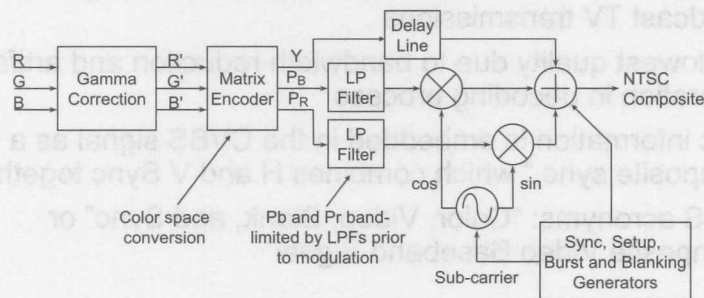
- **CVBS** combines the luma (brightness), chroma (color), blanking and sync information into one highly encoded analog signal
- Includes NTSC, PAL, and SECAM used in analog broadcast TV transmissions
- Has lowest quality due to bandwidth reduction and artifact generation in decoding process
- Sync information is embedded in the CVBS signal as a "composite sync," which combines H and V Sync together
- CVBS acronyms: "Color, Video, Blank, and Sync" or "Composite Video Baseband Signal"



Composite video is the most common analog video signal used in consumer video and broadcast TV. Composite video has been used in analog broadcast TV transmissions since the 1950's (NTSC) due to its low bandwidth and backward-compatibility with black-and-white TV sets. Now, digital TV signals make much better use of the broadcast spectrum. Analog TV is now slowly being replaced due to its inefficient use of the RF spectrum, inferior picture quality, and as more digital, high-definition content is produced. With analog broadcast TV going out of favor, composite video will most likely remain for non-broadcast video applications, such as low-end consumer video.

Implementation of NTSC Color Block Diagram

- NTSC system (and PAL) was devised to allow chroma information to be added to the luma signal in a manner transparent to monochrome TV for backward compatibility
- Basic parameters of the signal (carrier frequencies, bandwidths, modulation format, etc.) had to remain unchanged

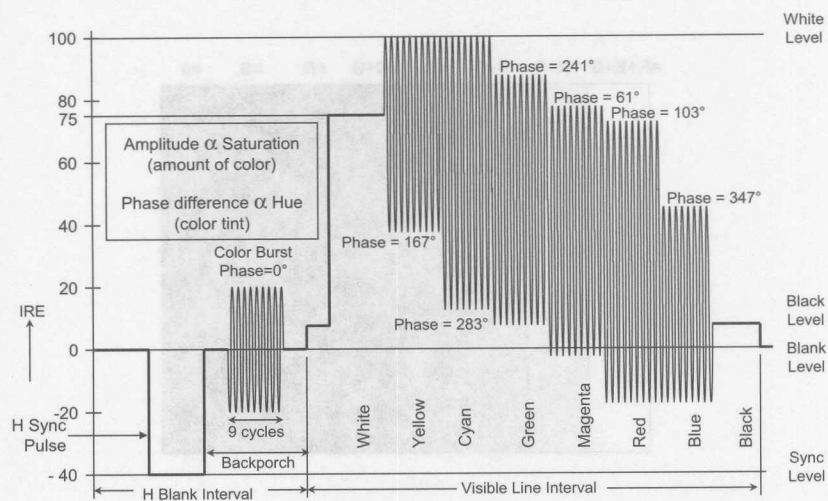


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In the PC/graphics space, RGB signals are used to make color. In the TV/video space, a different color space was developed to accommodate the need for backward compatibility with monochrome TV. A color or matrix encoder converts between the RGB and $Y P_B P_R$ color spaces. The difference signals (P_B , P_R) are band-limited using low-pass filters and used to modulate the amplitude and phase of the 3.58 MHz color subcarrier. This system takes advantage of the spectral nature of the luminance signal and the fact that the eye is less sensitive to color changes than luminance changes.

Sync, setup, burst, and blanking generators are added to the combined Y/C signal to produce the NTSC composite signal.

NTSC Video Signal (EIA 75% Color Bar Signal)

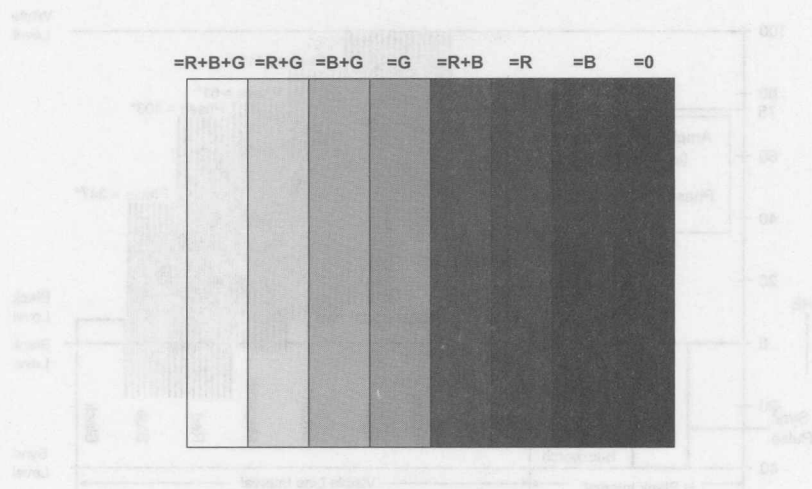


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This is a horizontal scan line of color bars. Color information is added on top of the luminance signal by the subcarrier waveform, with the color (or tint) identified by the phase difference between the subcarrier and the color-burst reference phase, and the amount of color (or saturation) conveyed by the amplitude of the subcarrier with respect to the color burst.

The horizontal blanking portion contains the horizontal synchronizing pulse (H sync pulse) as well as the color reference (color burst) located just after the rising edge of the sync pulse (called the back porch). The horizontal blanking portion of the signal is positioned in time such that it is not visible on a correctly adjusted display.

NTSC Video Pattern (EIA 75% Color Bar Signal)



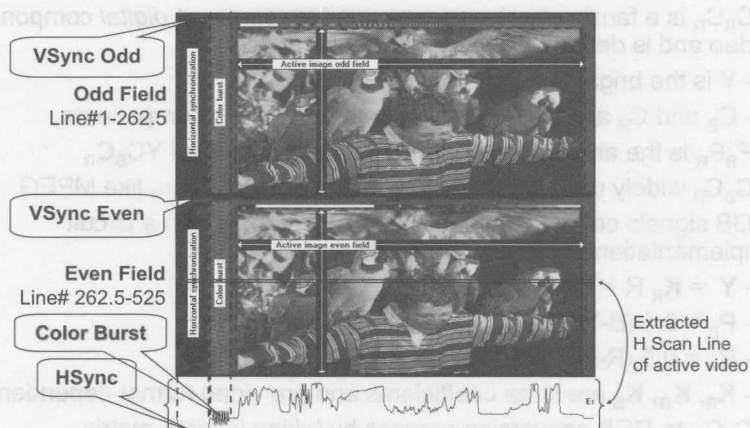
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This shows the resulting video pattern from the 75% color bar signal. In order from left to right, the colors are white, yellow, cyan, green, magenta, red, blue, and black. This sequence runs through all seven possible combinations that use at least one of the three basic color components of green, red, and blue.

Because green contributes the largest share of luminance, followed by red, then blue, this sequence of bars thus appears on a waveform monitor in luminance mode as a downward staircase from left to right.

Color bar patterns are commonly used to assist in the calibration of analog NTSC equipment in television network facilities.

NTSC Video and Sync Illustration

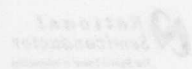


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This shows an example of two NTSC fields that comprise one frame. Each field begins with the vertical blanking interval (about 20 lines) before scanning the active video (viewable image) area, denoted by vertical and horizontal arrows. Each horizontal scan line begins with the horizontal sync and color burst signals before the video signal. The waveform shown at the bottom shows an extracted horizontal scan line of active video.

YP_BP_R: Analog Component Video

- YC_BC_R is a family of color spaces used to represent *digital* component video and is derived from the RGB color space
 - Y is the brightness or luma component
 - C_B and C_R are the Chroma or color-difference components
- YP_BP_R is the analog component video form of digital YC_BC_R
- YC_BC_R widely used for video and image compression, like MPEG
- RGB signals can be converted to YP_BP_R signals with a circuit implementation of the matrix equation:
 - $Y = K_R R + K_G G + K_B B$
 - $P_B = 0.5 (B-Y)/(1-K_B)$
 - $P_R = 0.5 (R-Y)/(1-K_R)$
 - K_R, K_G, K_B are luma coefficients and are video format dependent
- YC_BC_R-to-RGB conversion process by taking inverse matrix



In YP_BP_R, RGB is converted into brightness or luma signal (Y) and two color difference or chroma signals (P_B and P_R). CIE tests noted that human vision has less spatial acuity for color information than it does for brightness information. If RGB component video is re-coded as a channel of brightness (Y) and two color difference channels (P_B and P_R), the color difference data can be spatially reduced without the eye detecting that a change in color has taken place. Digital YC_BC_R is used widely in video and image compression schemes, like MPEG, due to its reduced bandwidth and storage requirements compared to three full-bandwidth channels of RGB.

Sometimes prime marks (') are associated with YP_BP_R or RGB (i.e.: Y'P_BP_R or R'G'B'). The prime marks refer to video signals that have gamma correction applied to correct for the non-linearity of phosphor CRT displays. In video systems, gamma correction is applied in the camera. Refer to the signal source to determine whether gamma correction is applied.

The YP_BP_R color space is produced by the linear addition and scaling of RGB, as shown in the matrix equation above.

YP_BP_R: Analog Component Video

- **SDTV Color Space: 480i/p** (per EIA-770.2)

$$-K_R = 0.299, K_G = 0.587, K_B = 0.114$$

- **HDTV Color Space: 720p/1080i** (per EIA-770.3)

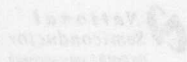
$$-K_R = 0.2126, K_G = 0.7152, K_B = 0.0722$$

- **Example: 480p matrix equations**

$$-Y = 0.299 R + 0.587 G + 0.114 B$$

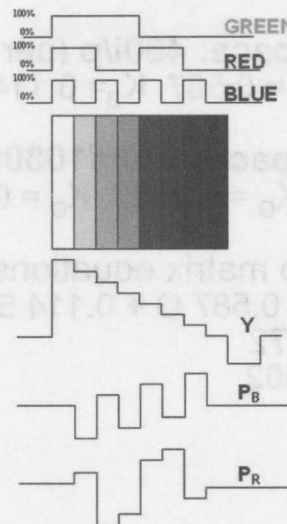
$$-P_B = (B - Y)/1.772$$

$$-P_R = (R - Y)/1.402$$



Luma coefficients are shown for SDTV and HDTV analog component color spaces, with the matrix equations shown for 480p.

$Y P_B P_R$: Color Space Conversion

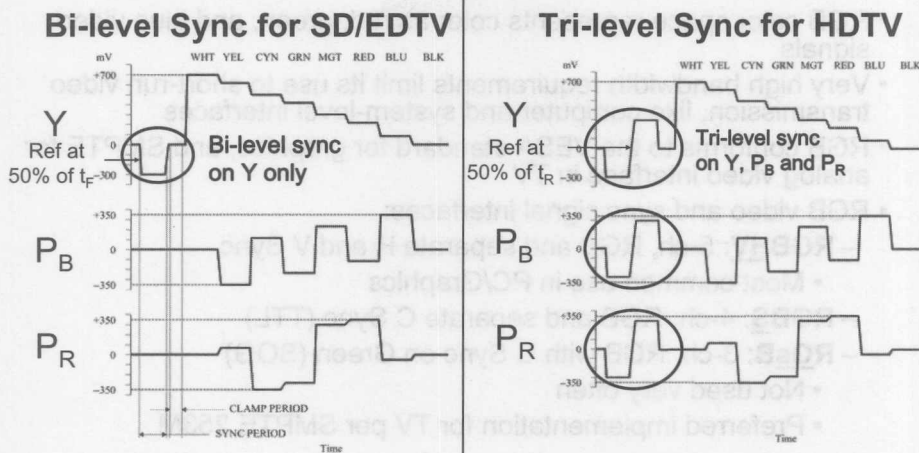


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Color is what is perceived by the human brain when the photoreceptors in the eyes are excited with a visual sensation. These colors can be interpreted or defined by specifications or models known as color spaces. Color is described using different color spaces, with each space associated to different applications based on system requirements and needs. RGB is an additive color system and its color space is defined by three components -red, green, and blue. It stems from the concept that the human eye is most sensitive to red, green, and blue, and all other colors are perceived as a combination of the three.

Color space conversion from the $Y P_B P_R$ color space to the RGB color space is shown here by taking the inverse of the matrix equation from the previous slide. RGB is very common, being used in virtually every computer system as well as video, etc. RGB is easy to implement, but non-linear with visual perception, and it is device dependent. Many other color spaces can be derived by applying linear functions of RGB. These color spaces separate RGB into luminance and chrominance information and are useful in compression applications (both digital and analog). These spaces are device dependent, but are intended for use under strictly defined conditions within closed systems. For example, television has adopted the more complex YUV color space in order to economize bandwidth for transmission and broadcast of its video signals.

Y_PB_PR: Sync Signals



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Bi-level sync is the standard sync signal method for all forms of standard-definition video. Systems using bi-level sync are typically negative edge-triggered. Bi-level sync, due to its asymmetry, introduces a DC component into the video signal, which can sometimes be problematic for sync separation.

Tri-level sync signal has faster rise times because of the increased bandwidth of HD, which results in more accurate timing edges, improving jitter performance, and sync separation. Symmetry of the tri-level sync signal eliminates the DC offset found in bi-level sync, which makes sync processing easier and more robust against noise. Tri-level sync appears on all three component signals.

The arrows indicate the sync threshold level and reference edge.

- Bi-level sync reference: 50% point on the negative-going edge.
- Tri-levels sync reference: 50% point on the positive-going edge of the tri-level sync, or a.k.a. positive-zero crossing.

RGB: PC/Graphics Video

- RGB color space represents color as red, green, and blue video signals
- Very high bandwidth requirements limit its use to short-run video transmission, like computer and system-level interfaces
- RGB conforms to the VESA standard for graphics, and SMPTE for analog video interface in TV
- RGB video and sync signal interfaces:
 - **RGBHV**: 5-ch, RGB and separate H and V Sync
 - Most common use in PC/Graphics
 - **RGBS**: 4-ch, RGB and separate C Sync (TTL)
 - **RGsB**: 3-ch, RGB with C Sync on Green (SOG)
 - Not used very often
 - Preferred implementation for TV per SMPTE 253M



RGB primary components are the native forms of analog video from a picture source, such as camera or telecine, or a synthetic RGB video from a PC or graphics generator, or a test signal generator. RGB's high-bandwidth requirement limits its use to local video transmission, like PC/graphics and other short-run, system-level video interfaces.

RGBHV has a total of five signals, red, green, blue, H Sync, and V Sync.

RGBS combines H and V sync into a single "composite sync" signal (S), resulting in a total of four signals.

RGsB or sync on green embeds the composite sync signal onto the green video signal for a total of three signals.

LMH1251

YP_BP_R-to-RGB Video Converter with Integrated 2:1 Video Switch

- First monolithic analog YP_BP_R video converter
- Precise YP_BP_R-to-RGBHV conversion for HDTV and SDTV
- Integrated 2:1 Video Switch
 - YP_BP_R Input Path
 - Converts 720p, 1080i, 1080p (HD) and 480i, 480p, 576i, 576p (SD)
 - Bi-level and tri-level sync plus Macrovision-compatible
 - RGBHV Input Path
 - Buffers RGBHV inputs up to UXGA (1600 x 1200 at 75 Hz)
- Auto format detection with SD/HD output flag
- Power-save mode
- 24-pin TSSOP package, small footprint, low component count



LMH1251 Key Specs

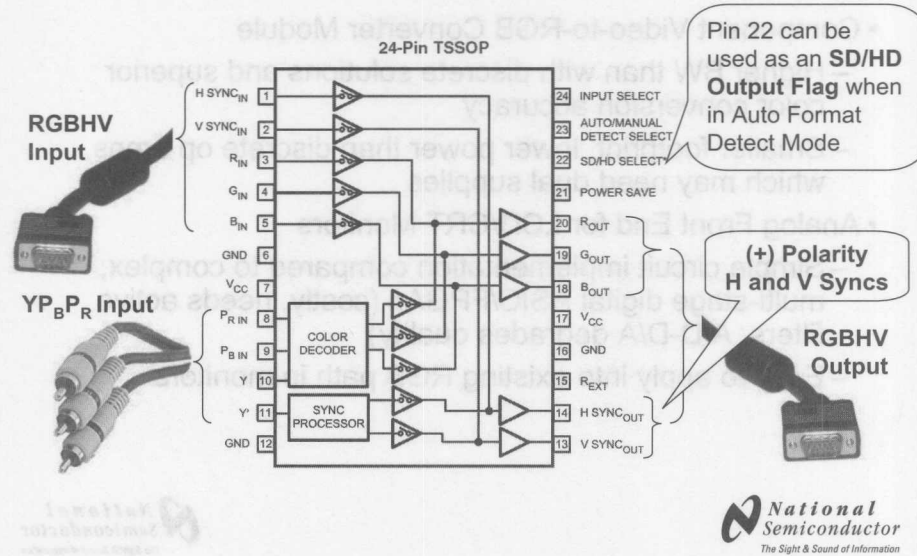
- Wideband Video Amplifiers
 - YP_BP_R Signal Path
 - 70 MHz Large-signal (700 mV_{P-P}) bandwidth
 - Superior chroma accuracy: Less than 2.5% differential gain and 1.5° differential phase
 - RGB Signal Path
 - 400 MHz Large-signal (700 mV_{P-P}) bandwidth
 - RGB output $t_R/t_F = 1.55$ ns for input $t_R/t_F = 1.5$ ns
- 5V supply operation
 - Typ. operating $I_{CC} = 70$ mA, 480p YP_BP_R input



Based on 1 V_{P-P} video inputs from a 75Ω analog video source.

The video conversion process is performed by a color-space conversion matrix using analog technology, rather than multiple stages of digital implementations. The result is a cleaner, crisper video image.

LMH1251 Connection Diagram



The internal sync separator strips off the sync component from the YP_BP_R input signal and generates the H and V sync signals, which are positive polarity logic outputs.

LMH1251 Applications

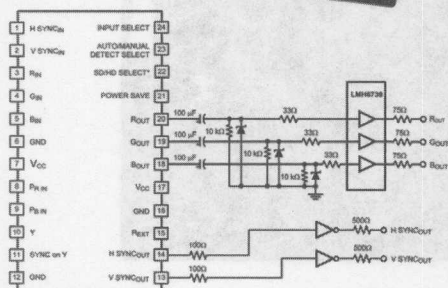
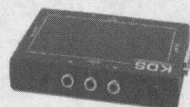
- Component Video-to-RGB Converter Module
 - Higher BW than with discrete solutions and superior color conversion accuracy
 - Smaller footprint, lower power than discrete op amps, which may need dual supplies
- Analog Front End for LCD/CRT Monitors
 - Simple circuit implementation compared to complex, multi-stage digital ASIC/FPGAs (costly, needs active filters, A/D-D/A degrades quality)
 - Easy to apply into existing RGB path in monitors



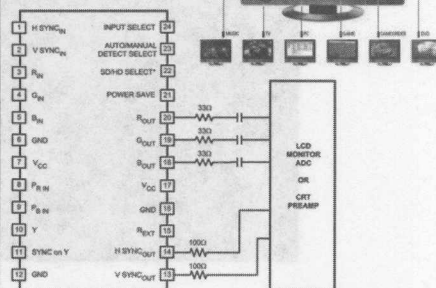
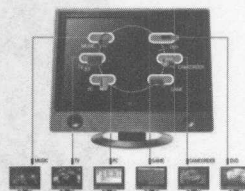
The LMH1251 is the first and only monolithic fully-analog YP_BP_R-to-RGB converter available. Discrete solutions using up to 20 components require design expertise, use more board space, consume more power and have inferior decoding quality. Digital solutions and FPGAs are more expensive and typically offer more features than may be needed in a system. Compared to these alternatives, the analog design of the LMH1251 reduces undesired artifacts and provides a smaller form factor for easy integration.

LMH1251 Applications

Component Video-to-RGB Converter Module with VGA Cable Driver



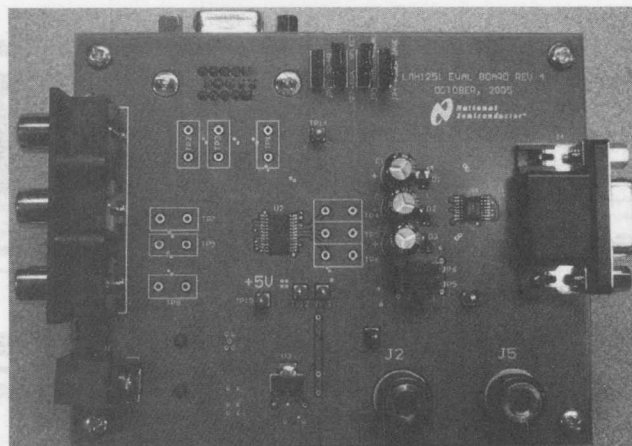
Video Front End for LCD Monitor ADC



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Example applications showing simplified application circuits.

LMH1251 Eval Board



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The LMH1251 evaluation boards, along with sample parts, are available for order on National's website.

Video Sync Separation

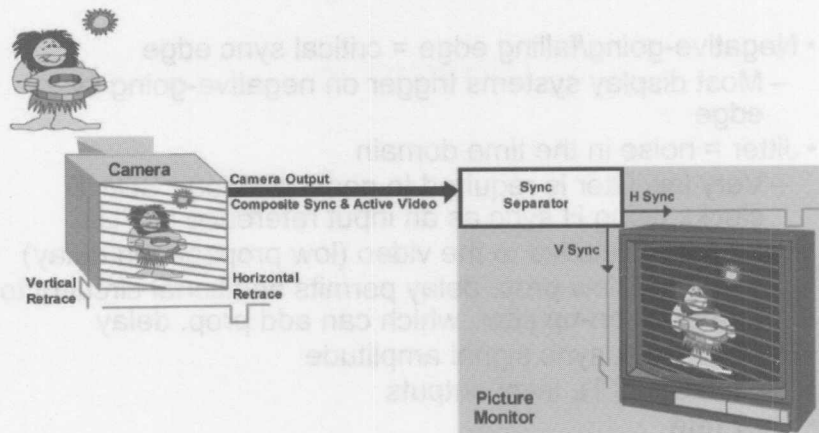
What is Sync and Why is it Important?

- Sync is critical to establish proper timing of RGB video content to its proper pixel locations in the image to generate a stable image on the display
- Without sync, image display isn't possible
- A display requires both horizontal (H) and vertical (V) sync:
 - H Sync regulates the scan line rate within a frame (or field).
 - V Sync defines the refresh rate for every frame (or field) of video.
- Different forms of sync signals:
 - ★– $Y P_B P_R$, Y/C, CVBS, RGsB: Composite sync embedded in the Y component, composite video, or G component in RGsB.
 - RGBHV: H and V carried as separate TTL sync signals
 - RGBS: H and V combined into a single TTL composite sync (S)



If two or more video sources are not in sync, a monitor will show rolling, tearing, or incorrect colors in the picture whenever a transition is made between sources.

Simplified Sync Illustration



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Critical Sync Output Characteristics

- Negative-going/falling edge = critical sync edge
 - Most display systems trigger on negative-going sync edge
- Jitter = noise in the time domain
 - Very low jitter is required to generate clean SD/HD clocks using H sync as an input reference to PLL
- Sync timing relative to the video (low propagation delay)
 - If needed, low prop. delay permits additional circuitry to further clean-up jitter, which can add prop. delay
- Peak-to-peak sync signal amplitude
 - CMOS or TTL level outputs
- Slew rate
 - Sync outputs with high slew rate necessary for low jitter



LMH1981 Key Features

- Sync separation for all standard analog video signals
 - **Formats:** 720p, 1080i (HDTV), 1080p, 480i/p, 576i/p (SD/EDTV), NTSC, PAL, SECAM, RGsB
 - **Signal Interfaces:** YP_BP_R (Component), Y/C (S-Video), CVBS (Composite), VGA (PC Graphics)
- Tri-level and bi-level sync compatible, Macrovision-compatible
- Precise 50% sync slicing ensures accurate sync separation
- Superior H sync jitter performance
- Automatic format detection and switching
 - No external programming via microcontroller, no power cycling required for video format switching
- Video format output (pin 9) – Binary coded line count o/p



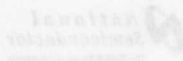
The LMH1981 is a multi-format sync separator with the industry's best jitter performance. It allows video designers to accurately and precisely extract horizontal and vertical sync signals without extra filtering and jitter-cleaning stages.

The LMH1981 is compatible with Macrovision video copy protection, in which pseudo sync pulses are embedded in the vertical blanking interval of the video signal – either recorded onto VHS tapes or created during playback by a chip on the DVD player. Other sync separators may mistake Macrovision pseudo sync pulses as true sync pulses, and react by outputting invalid sync signals.

Precise 50% sync slicing ensures accurate sync separation under varying input amplitude, offset, and noise conditions.

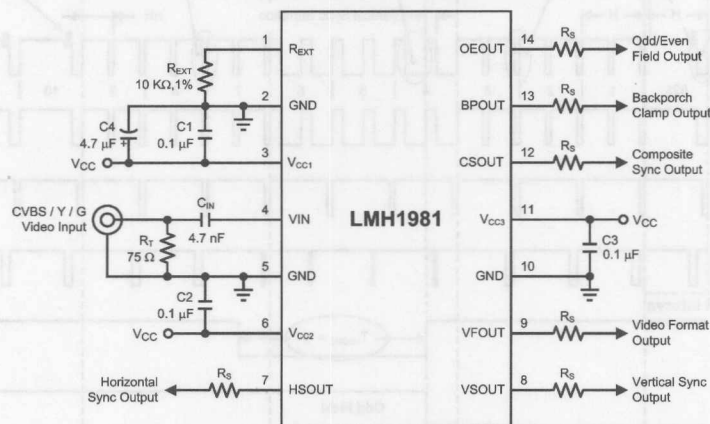
LMH1981 Key Specs

- 3.3V to 5V supply operation
 - 3.3V critical to match FPGA input voltage range
- 0.5 to 2 V_{P-P} video input range
 - Important for double or no 75Ω input termination conditions
- Typical H sync output jitter on *negative-going edge reference*
 - < 500 ps_{P-P} for HDTV (tri-level sync)
 - < 1000 ps_{P-P} for EDTV, RGsB
 - < 1500 ps_{P-P} for SDTV, CVBS
- Typical H sync prop. delay < 50 ns
- V Sync output pulse width = 3H
- 14-pin TSSOP package



LMH1981 Pinout and Test Circuit

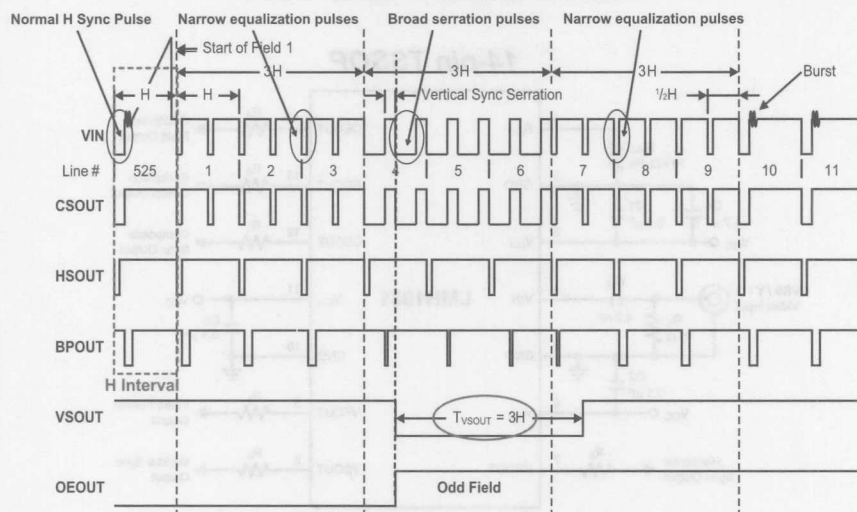
14-pin TSSOP



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The LMH1981 has three V_{CC} and three GND pins, one R_{EXT} pin, and six timing output pins. Very minimal BOM list: supply bypass caps, AC coupling cap to input, R_{EXT} 0.1% precision, series resistors on outputs for current-limiting during short-circuit conditions.

LMH1981 Vertical Interval NTSC – Odd Field



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NTSC employs a total of 525 horizontal lines per frame, with 2 fields per frame of 262.5 lines each. The odd field begins with a full line of video and ends with a half line of video.

VIN: NTSC vertical interval odd field shown in the top waveform with equalization and serration pulses over the first 9 H lines.

Vertical equalization and serration pulses are used to indicate the beginning of a new field for proper sync separation.

All outputs are in CMOS logic with rail-to-rail output range.

CSOUT: Composite sync output reproduces the input sync pulses with active video portion stripped off.

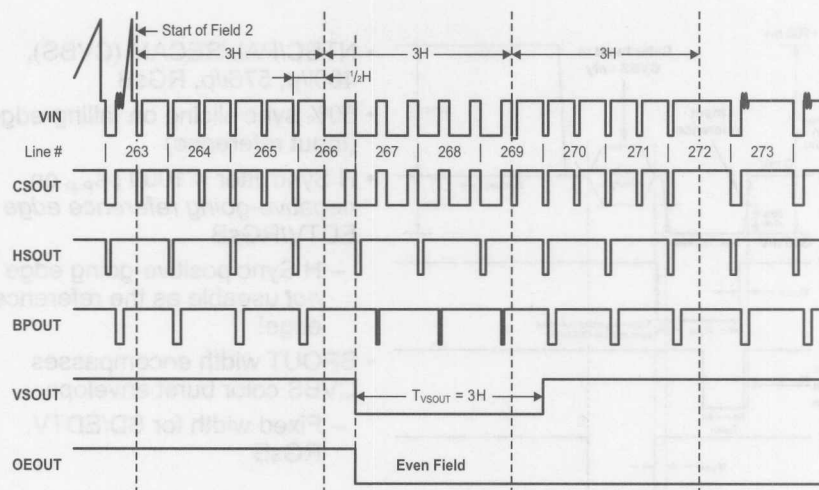
HSOUT: Horizontal sync output timing with the leading, falling-edge used as the reference edge.

BPOUT: Burst/back porch clamp output, triggered from the input sync rising edge, can be used as a timing signal for burst signal stripping and black level clamping (DC restoration).

VSOUT: Vertical sync output timing with V Sync pulse width of 3H's, with leading edge aligned with the first vertical serration pulse.

OEOUT: Odd/even field is high (or logic 1) for odd fields, edge aligned with V Sync leading edge.

LMH1981 Vertical Interval NTSC – Even Field



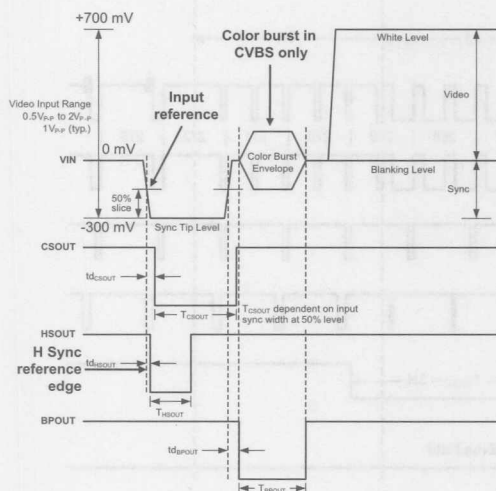
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The NTSC even field begins with a half line of video and ends with a full line.

VIN: NTSC vertical interval even field shown.

OEOUT: Odd/even field is low (or logic 0) for even fields.

LMH1981 Horizontal Interval Bi-Level Sync



- NTSC/PAL/SECAM (CVBS), 480i/p, 576i/p, RGsB
- 50% sync slicing on falling-edge (Input reference)
- H Sync jitter $< 1000 \text{ ps}_{\text{P-P}}$ on *negative-going reference edge* for EDTV/RGsB
 - H Sync positive-going edge *not* useable as the reference edge!
- BPOUT width encompasses CVBS color burst envelope
 - Fixed width for SD/EDTV, RGsB



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Color burst is present only in composite video signals.

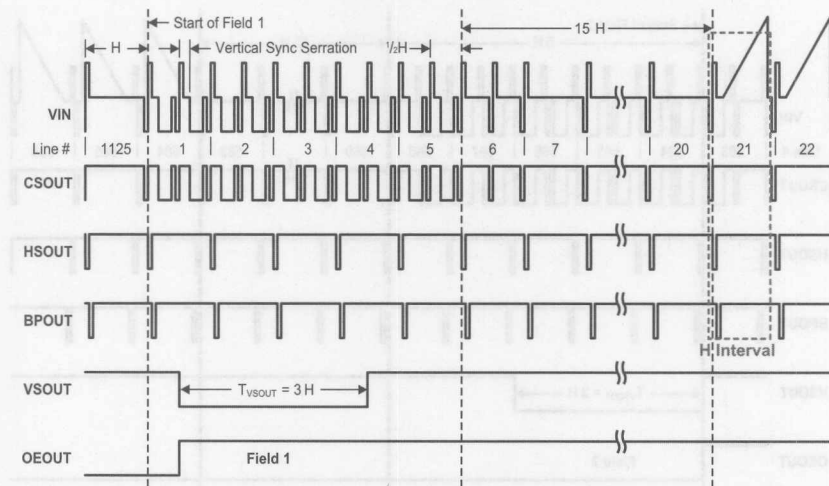
The H sync and C sync negative-going edges are triggered from the 50% level of the input sync negative edge (reference), each with prop delays.

The H sync negative-going edge has very low jitter and must be used as the reference edge for PLL inputs or display's synchronization systems.

Due to the narrow equalization pulses during the NTSC vertical interval period, the H sync output positive-going edges are “reconstructed” by the ICs internal timing. Therefore, the H sync rising edge must not be used as the reference edge.

The back porch output is derived from the input sync trailing edge with a prop delay.

LMH1981 Vertical Interval 1080i – Field 1 (SMPTE 274)



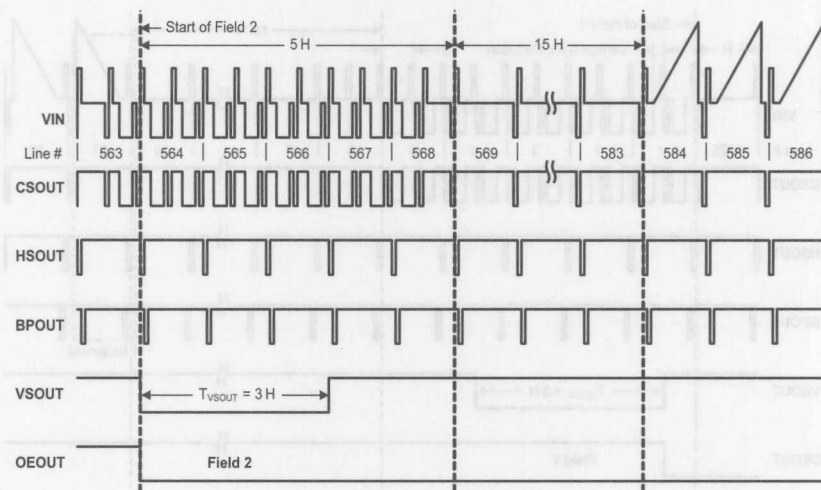
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1080i employs a total of 1125 horizontal lines per frame, with 2 fields per frame of 562.5 lines each.

CSOUT: Composite sync output reproduces the input sync pulses below the video blanking level (0 mV).

OEOUT: Odd/even field is logic high (or logic 1) for field 1.

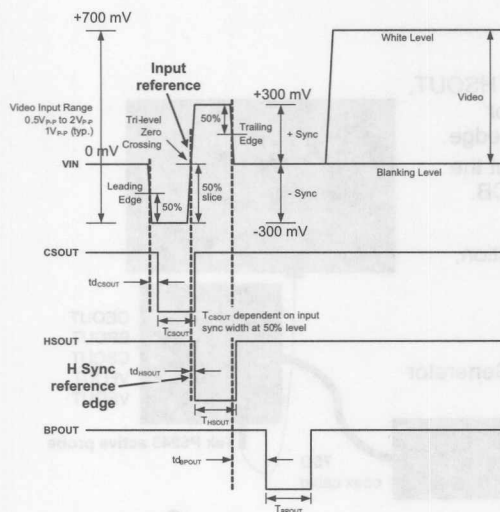
LMH1981 Vertical Interval 1080i – Field 2 (SMPTE 274)



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OEOUT: Odd/even field is logic low (or logic 0) for field 2.

Horizontal Interval HDTV Tri-Level Sync



- 720p, 1080i
- 50% sync slicing at tri-level zero crossing (Input reference)
- H Sync jitter < 500 ps_{P-P} on negative-going edge reference for HDTV
- CSOUT delay from input leading-edge
- HSOUT delay from tri-level zero crossing
- BPOUT delay from input trailing-edge

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The timing diagram shows the HD tri-level sync that precedes the active video signal.

The C sync negative-going, leading edge is triggered from the 50% level of the input sync's negative-going, leading edge with a prop delay.

The H sync negative-going, leading edge has very low jitter and must be used as the reference edge for PLL inputs or display's synchronization systems.

The H sync leading edge is triggered from the input sync's tri-level zero-crossing (reference).

The back porch output is derived from the input sync's negative-going, trailing edge with a prop delay.

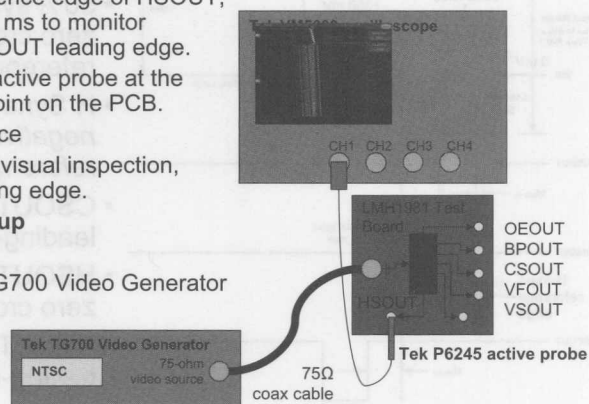
H Sync Accumulated Jitter Test Measurement Setup

VM5000 Oscilloscope Setup

- Triggered on 50% reference edge of HSOUT, with horizontal delay ~20 ms to monitor *accumulated jitter* on HSOUT leading edge.
- CH1 has a Tek P6245 active probe at the LMH1981 HSOUT test point on the PCB.
- 4 sec. display persistence
- Pk-Pk jitter obtained by visual inspection, zoomed into HSOUT falling edge.

LM1981 Test Board Setup

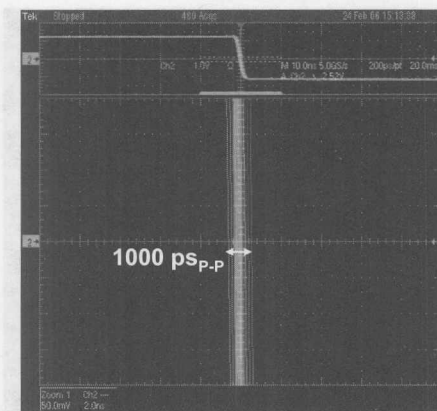
- $V_{CC} = 5V$
- Video input from Tek TG700 Video Generator



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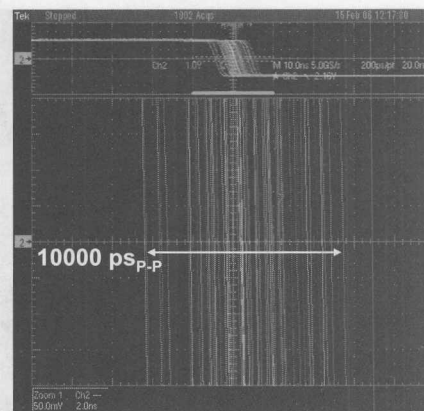
LMH1981 vs competitor at NTSC H Sync Output Typical Jitter

LMH1981



Zoom scale: 50 mV/div, 2 ns/div

Competitor



* digital filter off

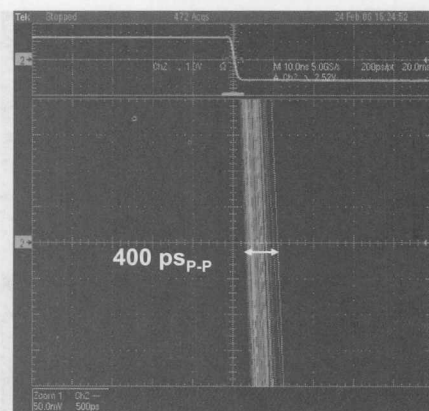


This slide shows the LMH1981 versus the closest competitor for jitter on H sync negative-going, reference edge for NTSC input.

Low jitter is critical for generating SD/HD video reference clocks for A/D conversion and SDI serializers.

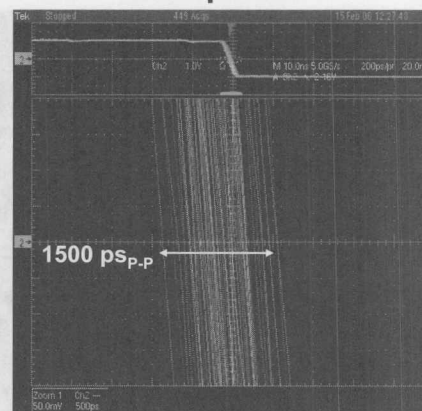
LMH1981 vs Competitor at 1080i H Sync Output Typical Jitter

LMH1981



Zoom scale: 50 mV/div, 2 ns/div

Competitor



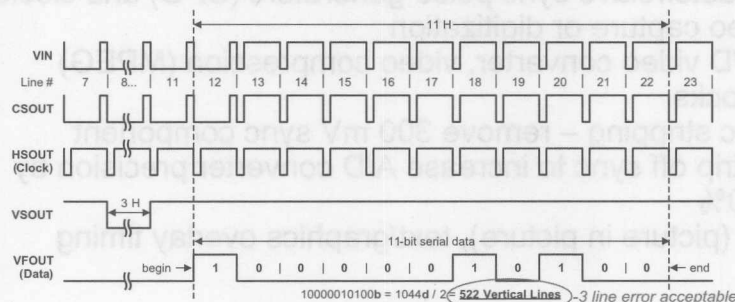
* digital filter off

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Here is the LMH1981 versus its closest competitor for jitter on H sync negative-going, reference edge for 1080i input.

Video Format Output Feature Example: 480p (525 total lines)

- Counts the # of H sync pulses per field and automatically doubles it (2 fields/frame) to approximate the total vertical scan line count
- Total vertical line count is output to VFOUT (pin 9) as an 11-bit binary coded bitstream, clocked out on the 11 consecutive falling edges of HSOUT after each VSOUT trailing edge
- Current solutions rely on FPGA resources to perform line count processing



11-bit binary data can be loaded into a serial-to-parallel shift registers and used by the FPGA for video format identification, enabling dynamic adjustment of video system parameters (like color space or scalar conversion).

Broadcast Video Applications

- Genlock – generator lock to house timing reference
 - Video camera, video tape recorder (VTR), time base controller (TBC), production switcher, frame synchronizer
- SD/HD clock and sync pulse generation
 - Master/slave sync pulse generators (SPG) and clocks
- Video capture or digitization
 - A/D video converter, video compression (MPEG) clocks
- Sync stripping – remove 300 mV sync component
 - Strip off sync to increase A/D converter precision by 30%
- PIP (picture in picture), text/graphics overlay timing

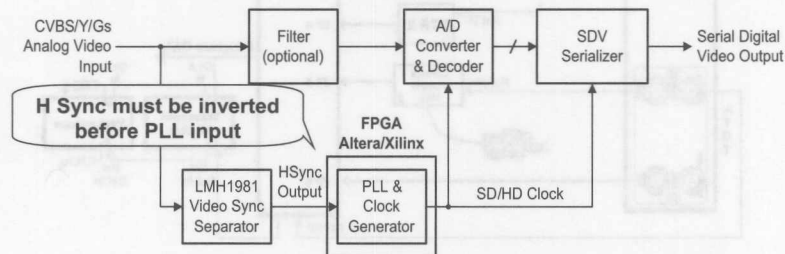


Synchronization is one of the most fundamental and critical procedures in a video facility. Every device in a system must be synchronized in order to successfully create, transmit, and recover pictures and audio information. The complexities of analog and digital multi-standard and multi-format environments require the flexibility to achieve and maintain synchronization in facilities that operate in a mix of video formats. As the broadcast TV industry begins to incorporate more high-definition programming, there will be a need to bridge the gap between analog and digital TV formats. The LMH1981 fills that gap by supporting all standard analog SDTV and HDTV formats.

Sync stripping of -300 mV sync component increases the ADC's dynamic range and hence ADC precision, by 30%.

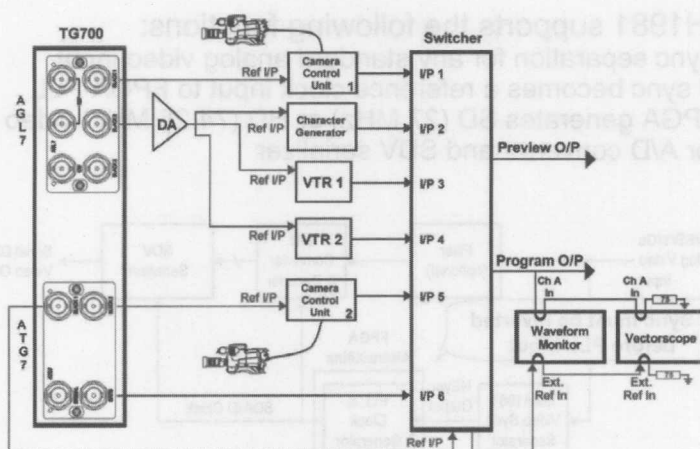
LMH1981 Application: Analog-to-SDV Video Converter

- LMH1981 supports the following functions:
 - Sync separation for any standard analog video input
 - H sync becomes a reference clock input to FPGA PLL
 - FPGA generates SD (27 MHz) or HD (74.25 MHz) video clocks for A/D converter and SDV serializer



Since the LMH1981 jitter is optimized for the H sync negative-going edge and most FPGA PLL inputs are rising-edge triggered systems, the H sync output must be inverted by the FPGA before the PLL input.

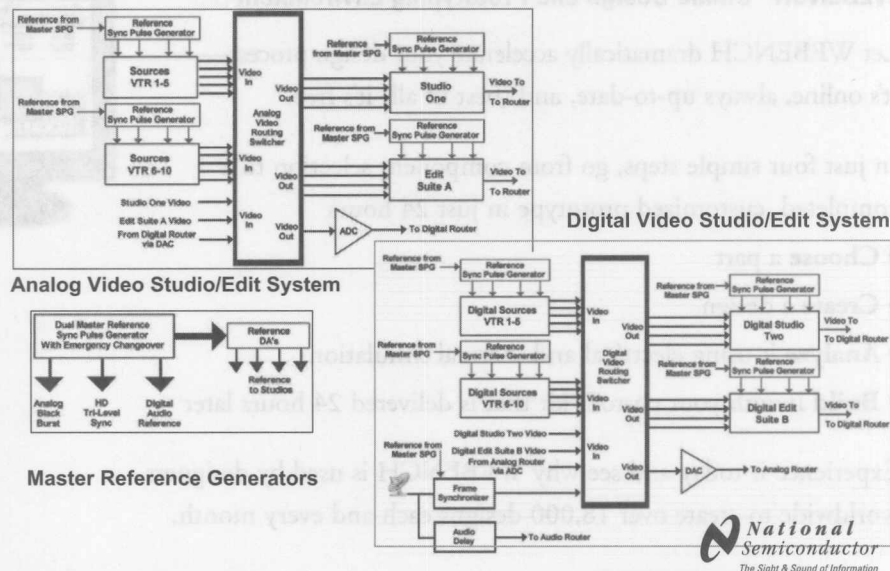
Example: Analog Video Studio System Using TG700



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A TV reference signal generator, such as the TG700, provides a "house reference" signal (composite black burst signal) to synchronize all analog broadcast video equipment, including cameras, character generators, Video Tape Recorders (VTR), and production switcher. Each piece of equipment needs to separate the syncs from the black burst signal, in order to extract the H and V sync and other timing information for proper sync. The LMH1981 can be used in various analog broadcast video equipment.

Multi-format Hybrid Facility



Newer multi-format, multi-standard hybrid video facilities have separate analog and digital video studio "islands." Video conversion is necessary before video from one island is routed to another island. For example, in order for analog video to be routed to the digital island, it must be digitized. The LMH1981 H sync output can be used to generate SD/HD reference clocks used in the video digitization process (A-D conversion). The LMH1981 also can be used in master sync pulse generators (SPG) and master clock systems, which are used to synchronize various broadcast equipment.

Design Tools

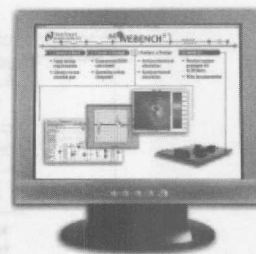
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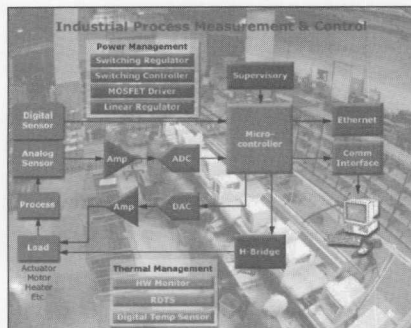
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PO Box 58090
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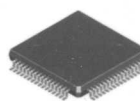

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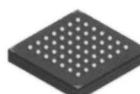

SOT-23



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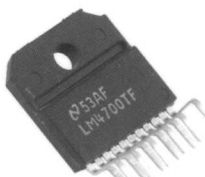

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SOIC


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